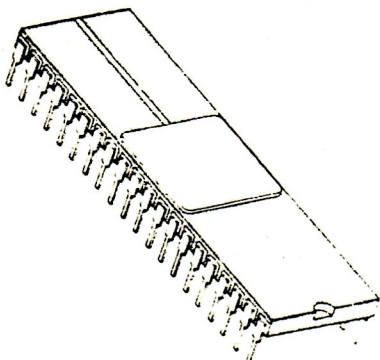


FILE:
MICROPROCESSOR
SYSTEMS
DEVICES

DATA SHEET **BELLMAC*8 MICROPROCESSOR**
212 SERIES



APPROXIMATE SIZE

DESCRIPTION

The **BELLMAC-8** microprocessors (212B, C, D, and E) are single-chip, bus structured, general purpose central processing units (CPUs) with 8-bit data and 16-bit address buses, packaged in a hermetically sealed 40-pin DIP. Logic elements are fabricated using one of three techniques: CMOS, pseudo NMOS with PMOS load devices, and dynamic NMOS logic arrays. An appropriate mix of these three techniques has yielded a functionally dense design while maintaining low power and high speed objectives (see **FEATURES**). The **BELLMAC-8** microprocessor has extensive addressing modes that result in a symmetric and flexible instruction set. Memory byte and instruction requirements of the instructions depend on the mode and not the function itself. The device requires a 12 volt dc supply for internal circuitry and a 5 volt dc supply for TTL compatibility on I/O pins.

FEATURES

- Powerful and Extensive Instruction Set
- 8-Bit Data and 16-Bit Address Buses
- 8-and 16-Bit Operations
- 65,536 Bytes of Direct Memory or I/O Addressing
- Direct Memory Access (DMA)
- Low Power Consumption
- 212B — DC to 2.06 MHz Clock (0 - 85°C) 380 mW typical power
- 212C — DC to 1.9 MHz Clock (0 - 75°C ambient) 350 mW typical power
- 212D — DC to 2.22 MHz Clock (0-85°C) 390 mW typical power; tighter tolerances suitable for Lock-Step Operation
- 212E — DC to 3.0 MHz Clock (- 40°-85°C) 480 mW typical power

USER INFORMATION

The microprocessor central processing unit (CPU) contains the circuitry needed to access memory locations and to decode and execute instructions. The CPU contains:

- An arithmetic logic unit (ALU) that performs arithmetic and logical operation.
- Two programmed logic arrays forming the CPU control section. The instruction control logic array (ICLA) directs the CPU through instruction execution states; the ALU control logic array (ACLA) controls ALU operation and latches ALU generated condition flags.

*Trademark of Western Electric
 §At 85°C the maximum frequency is 1.85 MHz
 EOL (end of life).

FUNCTIONAL BLOCK DIAGRAM

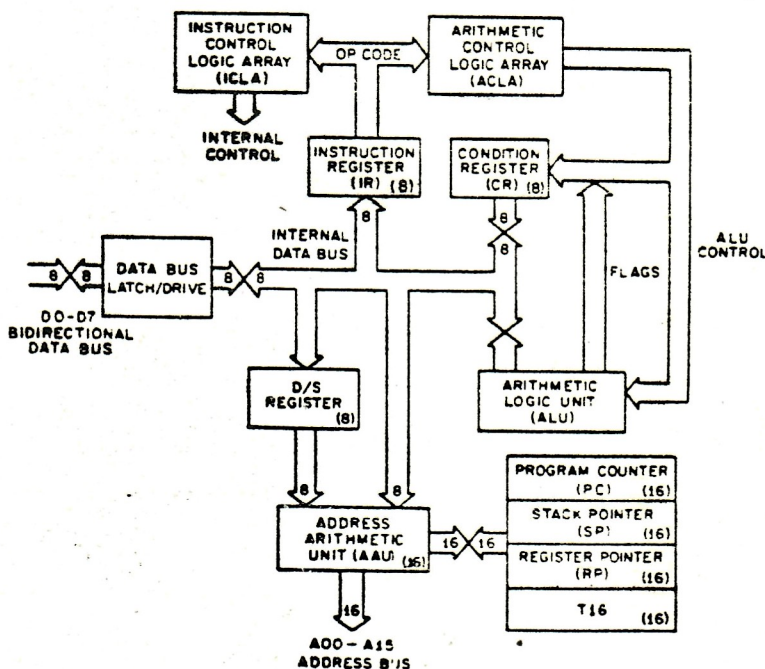


FIGURE 1

INFORMATION (Cont'd)

- An address arithmetic unit (AAU) performs address calculations.
- On-chip registers for temporarily storing data, addresses, and instructions (these are not general purpose data manipulation registers):
 - ▶ Program Counter (PC) - contains the 16-bit memory address of the instruction byte being executed or, upon instruction completion, contains the starting address of the next instruction to be executed.
 - ▶ Instruction Register (IR) - contains the instruction being executed (8-bits).
 - ▶ Condition Register (CR) - contains 8-bits that indicate conditions resulting from the operation just completed. A program instruction can test for the presence or absence of a condition to select the next instruction to be executed.
 - ▶ D/S Register - stores two 4-bit qualifiers, one for the destination (D) and the other for the source. These qualifiers are used for determining the address of the destination and source operands. i.e., where in memory to find the data to be used in the operation and where to store the results.
 - ▶ Register Pointer (RP) - contains the starting address in read/write memory (RAM) of sixteen 16-bit general purpose registers.
 - ▶ Stack Pointer (SP) - contains the current 16-bit memory address of the pushdown stack, i.e., the memory address of the last item stored (pushed) on the stack or of the next item to be retrieved (popped) from the stack.
 - ▶ Register T16 - a 16-bit register used as a scratchpad during address calculations.

The microprocessor is byte-oriented. The instruction repertoire includes logical and arithmetic operations on 8 and 16-bit quantities, supplemented by 16-bit operations chosen to facilitate address arithmetic. A 16-bit address bus provides for addressing of up to 65,536 bytes of memory.

The microprocessor uses a set of 16 identical 16-bit general purpose working registers located in external memory (RAM) for indexing (addressing) or as accumulators. These registers, together with addressing modes, form a highly symmetrical set of operand combinations for the instructions.

A last-in/first-out pushdown stack, locatable in any portion of the 65,536 bytes of addressable memory space, is used as the subroutine call/return mechanism, to save and restore processor status during interrupts, and to allow dynamic storage management. The programmer controls the amount of memory allocated to the stack which, in turn, determines how many interrupts and subroutines can be nested at any point in a program.

The 8-bit condition register (CR) indicates program status at any given point in its execution. The bits in the CR describe the results of the most recent arithmetic or logical instructions and can be tested using the condition instructions to control decision making and branching during program execution. Bits 0→7 comprise the CR; bits 8→15 represent testable conditions derived from the first eight bits and do not physically exist in any register. See MICROPROCESSOR CONDITIONS—Table 1.

CPU AND RAM REGISTERS

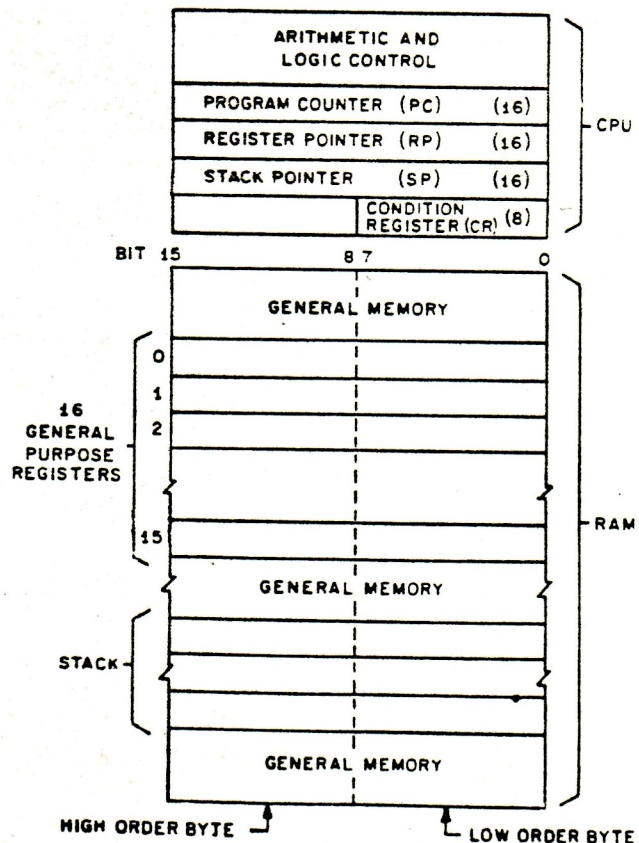


FIGURE 2

USER INFORMATION (Cont'd)

GENERAL REGISTER STRUCTURE

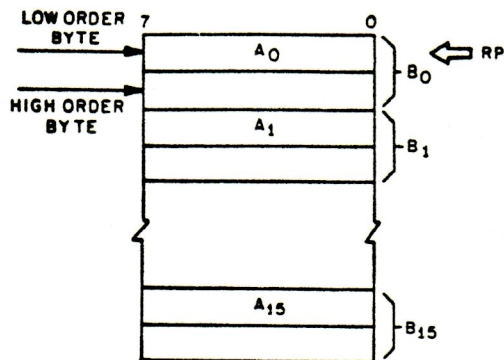


FIGURE 3

BELLMAC-8 MICROPROCESSOR CONDITIONS

BIT	TEST CODE [ⓐ]	CLEARED (0)	SET (1)	DESCRIPTION	REMARKS
0	0	!neg	neg	Sign bit of result	ACTUAL CONDITION REGISTER BITS
1	1	!zero	zero	Indicates all zero result	
2	2	!ovfl	ovfl	Indicates arithmetic overflow	
3	3	!carry	carry	Indicates carry of borrow	
4	4	!ones	ones	Indicates result is all ones	
5	5	!odd	odd	Lower-order (LSB) of result	
6	6	!enable	enable	Interrupts are enabled	
7	7	!flag	flag	User-designated flag	
8	8	!lt	lt	Arithmetically less than zero (bit 0⊕bit 2)	DERIVED FROM CONDITION REGISTER BITS 0-7 (NOT PART OF CONDITION REGISTER)
9	9	!lteq	lteq	Arithmetically less than or equal to zero [(bit 0⊕bit 2) bit 1]	
10	A	!lteq	lteq	Logically less than or equal to zero (bit 3 bit 1)	
11	B	!homog	homog	Logically homogeneous (all zeros or all ones) (bit 4 bit 1)	
12	C	!shovfl	shovfl	Arithmetic left-shift overflow (bit 0⊕bit 3)	
13	—	—	—	(Unused, Unassignable)	
14	—	—	—	(Unused, Unassignable)	
15	F	—	always	Condition always true (set) (unconditional jump, call, return)	

! nontrue condition

⊕ bit-by-bit exclusive OR

| bit-by-bit inclusive OR

ⓐ Test code is the hexadecimal value entered into instruction used to test ER.

TABLE 1

ADDRESSING MODES

The addressing modes of an instruction are the different ways in which the effective address of the operands of the instruction are formed. Instructions that do not address memory do not have addressing modes.

For instructions that have an addressing mode, the first instruction byte contains 2 or 3 bits reserved for the mode indicator. Monadic instructions involve a single operand called the destination (d) and have a 2-bit mode indicator. Dyadic instructions have both a source (s) and a destination (d) operand and use a 3-bit mode indicator.

The addressing mode tables identify the modes of addressing operands in monadic and dyadic instructions. The columns indicate the addressing mode, hexadecimal code indicator, and register number range for the destination/source byte (d/s operand qualifiers).

Single-Operand Instructions:

The 8-bit monadic instructions can use any of these addressing modes. The 16-bit monadic instructions can use only the Register mode (code 0). The operand qualifier occupies the d field of the d/s byte; the s field is not used here for addressing.

MONADIC ADDRESSING MODES

Address Mode Destination	Mode Code	Register Range d
Register	0	0-15
Indirect	1	0-14
Direct	1	15
Offset Memory	2	0-14
Offset Stack	2	15
Auto Increment	3	0-15

TABLE 2

The 16 general-purpose registers can be located in any 32-byte section of available RAM and can be accessed in two different ways:

- As a 16-bit base register (B register) used primarily to hold a memory address.
- As a low-order, 8-bit accumulator (A register) for arithmetic and logic operations.

The first two bytes of this section are register 0, the next two are register 1, etc. The starting address of this section is contained in the 16-bit register pointer (RP). The register set can be relocated to any 8-byte boundary (starting address divisible by 8) in memory by changing the contents of the RP.

ADDRESSING MODES (Cont'd)

DYADIC ADDRESSING MODES

Address Mode		Mode Code	Register Range	
Destination	Source		d	s
Register	Register	0	0-15	0-14
Register	Immediate	0	0-15	15
Indirect	Register	1	0-14	0-14
Indirect	Immediate	1	0-14	15
Direct	Register	1	15	0-14
Direct	Immediate	1	15	15
Offset Memory	Register	2	0-14	0-14
Offset Memory	Immediate	2	0-14	15
Offset Stack	Register	2	15	0-14
Offset Stack	Immediate	2	15	15
Auto Increment	Register	3	0-15	0-15
Auto Increment	Immediate	3	0-15	15
Offset Memory	Offset Memory	4	0-14	0-14
Offset Memory	Offset Stack	4	0-14	15
Offset Stack	Offset Memory	4	15	0-14
Offset Stack	Offset Stack	4	15	15
Register	Indirect	5	0-15	0-14
Register	Direct	5	0-15	15
Register	Offset Memory	6	0-15	0-14
Register	Offset Stack	6	0-15	15
Register	Auto Increment	7	0-15	0-15

TABLE 3

Two-Operand (Dyadic) Instructions:

The table lists the addressing modes for the destination and source operands. However, mode 4 is **not** available for 16-bit dyadic instructions.

OPCODE ASSIGNMENTS

The OPCODE ASSIGNMENTS table lists the function assigned to the available microprocessor opcodes (hexadecimal 00 through FF or binary 00000000 through 11111111). Blank entries in the FUNCTION column identify currently unassigned opcodes. If a range appears in the HEX column, the mode indicator (denoted by xx or xxx in the Binary column) is added to the lowest number in the range to determine the opcode for that function; where xx is any monadic mode number (0 to 3) and xxx is any dyadic mode number. Mode 4 (memory-to-memory) can be used only for 8-bit instructions and the 8-bit instructions uses the opcode for the corresponding 16-bit instructions. Opcodes for mode 4 in the 8-bit instruction group are not used.

The COND column entry identifies the effect that function has on the Condition Register and indicates the valid result. The COND characters denote the following:

0 Alters negative bit	4 Alters ones bit	M Mask determines conditions affected
1 Alters zero bit	5 Alters odd bit	N No effect; conditions unchanged
2 Alters overflow bit	6 Alters enable bit	S Byte popped from stack determines conditions affected
3 Alters carry bit	7 Alters flag bit	

Refer to the MICROPROCESSOR CONDITIONS table for additional information.

The "odd ones" and "even ones" bits are affected by all 16-bit dyadic instructions (move, OR, XOR, AND subtract, add, compare) and the 16-bit increment and decrement instructions in an undefined manner.

The TYPE column indicates whether the instruction is monadic (M) or dyadic (D). The Mode column indicates the addressing mode(s) legal for the instruction or instruction range. The BYTES and CYCLES columns give the length of the instruction in memory bytes and machine cycles, respectively.

Unassigned opcodes are illegal and will cause the microprocessor to trap.

OPCODE ASSIGNMENTS

HEX	FUNCTION	BINARY	TYPE	MODE(S)	COND	BYTES	CYCLES
00	Illegal Opcode	00000000			N		
01	Set Conditions	00000001			M	2	5
02		00000010					
03	Clear Conditions	00000011			M	2	5
04	POP A	00000100	M	0	N	2	7
05	POP CR	00000101			S	1	7
06	PUSH A	00000110	D(s)	0	N	2	6
07	PUSH CR	00000111			N	1	6
08		00001000					
09		00001001					
0A		00001010					
0B		00001011					
0C	Find Left One	00001100	D, 8 bit	0	0,1,4,5	2	8
0D	Load SP	00001101			N	2 or 4	8
0E	Count Ones	00001110	D, 8 bit	0	0,1,4,5	2	8
0F		00001111					
10-13		000100xx					
14-17		000101xx					
18-1B		000110xx					
1C-1F		000111xx					
20-23	Zero	001000xx	M, 8 bit	0-3	0,1,4,5	2 to 4	8 to 14
24-27	Negate	001001xx	M, 8 bit	0-3	0,1,2,3,4,5	2 to 4	8 to 14
28-2B	Increment/Decrement	001010xx	M, 8 bit	0-3	0,1,2,3,4,5	2 to 4	8 to 14
2C-2F	Complement	001011xx	M, 8 bit	0-3	0,1,4,5	2 to 4	8 to 14
30-33	Shift Arithmetic	001100xx	M, 8 bit	0-3	0,1,2,3,4,5	2 to 4	8 to 14
34-37	Rotate 8	001101xx	M, 8 bit	0-3	0,1,2,3,4,5	2 to 4	8 to 14
38-3B	Shift Logical	001110xx	M, 8 bit	0-3	0,1,2,3,4,5	2 to 4	8 to 14
3C-3F	Rotate 9	001111xx	M, 8 bit	0-3	0,1,2,3,4,5	2 to 4	8 to 14
40	Branch 2 False	01000000	M	2	N	3	6 to 8
41	Branch 1 False	01000001	M	1	N	2 or 4	6 or 7
42	Bump 4	01000010			N	1	6
43	Bump 8	01000011			N	1	6
44	POP B	01000100	M	0	N	2	10
45	POP RP	01000101			N	1	9
46	PUSH B	01000110	D(s)	0	N	2	10
47	PUSH RP	01000111			N	1	8
48	Branch 2 True	01001000	M	2	N	3	6 to 8
49	Branch 1 True	01001001	M	1	N	2 or 4	6 or 7
4A	Debump 4	01001010			N	1	6
4B	Debump 8	01001011			N	1	6
4C	Find & Clear Left One,	01001100	D, 8 bit	0	0,1,4,5	2	11
4D	Load RP	01001101	D(s), 16 bits	0	N	2 or 4	8
4E		01001110					
4F		01001111					

(s) Source

xx any monadic mode number (0 to 3)

TABLE 4

OPCODE ASSIGNMENTS

HEX	FUNCTION	BINARY	TYPE	MODE(S)	COND	BYTES	CYCLES
50		01010000					
51		01010001					
52	Branch on Reg Bit False	01010010	D	2/2a (s/d)	N	3	8 or 7
53	Branch on Mem Bit False	01010011	D	5/2a (s/d)	N	3	11 or 10
54		01010100					
55		01010101					
56		01010110					
57		01010111					
58	Branch 2	01011000	M	2a	N	2	5
59	Branch 1	01011001	M	1a	N	3	6
5A	Branch on Reg Bit True	01011010	D	2/2a (s/d)	N	3	8 or 7
5B	Branch on Mem Bit True	01011011	D	5/2a (s/d)	N	3	11 or 10
5C		01011100					
5D		01011101					
5E		01011110					
5F		01011111					
60	Zero 16	01100000	M	0	0,1,4,5	2	12
61	Call False	01100001	M	1	N	2 or 4	11-12 or 6-7
62	Sign Extend	01100010	M	0	N	2	6
63		01100011					
64	Sub Return True	01100100			N	2	8 or 7
65	Sub Return False	01100101			N	2	8 or 7
66	Sub Return	01100110			N	1	8
67	Interrupt Return	01100111			S	1	9
68	Increment/Decrement 16	01101000	M	0	0,1,2,3,4,5	2	12
69	Call True	01101001	M	1	N	2 or 4	11-12 or 6-7
6A	Swap Bytes	01101010	M	0	N	2	9
6B		01101011					
6C		01101100					
6D	Load Register Address	01101101	D	0	N	2	9
6E		01101110					
6F	Load Address	01101111	D	6	N	3	13
70		01110000					
71		01110001					
72		01110010					
73	Branch on Mem Bit False††	01110011	D	7/2a (s/d)	N	3	14
74		01110100					
75	Add 8 Bits Logical	01110101	D	0†	N	2 to 3	10 or 14
76		01110110					
77		01110111					
78	Halt	01111000			6 (Set)	1	4 (min)
79	Call	01111001	M	1	N	3	11
7A		01111010					
7B	Branch on Mem Bit True††	01111011	D	7/2a (s/d)	N	3	14
7C		01111100					

†† Post increment of address

s/d source/destination

a abbreviated

OPCODE ASSIGNMENTS

HEX	FUNCTION	BINARY	TYPE	MODE(S)	COND	BYTES	CYCLES
7D 7E 7F	Add 8 Bits Arithmetic NOP	01111101 01111110 01111111	D	0†	N N	2 to 3 1	10 or 14 4
80-83 84 85-87 88-8B 8C 8D-8F	Move Move XOR XOR	10000xxx 10000100 10000xxx 10001xxx 10001100 10001xxx	D, 8 bit D, 8 bit D, 8 bit D, 8 bit	0-3 5-7 0-3 5-7	0,1,4,5 0,1,4,5 0,1,4,5 0,1,4,5	2 to 5 2 to 4 2 to 5 2 to 4	9 to 16 12 to 15 9 to 16 12 to 15
90-93 94 95-97 98-9B 9C 9D-9F	OR OR AND AND	10010xxx 10010100 10010xxx 10011xxx 10011100 10011xxx	D, 8 bit D, 8 bit D, 8 bit D, 8 bit	0-3 5-7 0-3 5-7	0,1,4,5 0,1,4,4 0,1,4,5 0,1,4,5	2 to 5 2 to 4 2 to 5 2 to 4	9 to 16 9 to 15 9 to 16 9 to 15
A0-A3 A4 A5-A7 A8-AB AC AD-AF	Subtract Subtract Add Add	10100xxx 10100100 10100xxx 10101xxx 10101100 10101xxx	D, 8 bit D, 8 bit D, 8 bit D, 8 bit	0-3 5-7 0-3 5-7	0,1,2,3,4,5 0,1,2,3,4,5 0,1,2,3,4,5 0,1,2,3,4,5	2 to 5 2 to 4 2 to 5 2 to 4	9 to 16 9 to 15 9 to 16 9 to 15
B0-B3 B4 B5-B7 B8-BB BC BD-BF	Compare Compare Test Test	10110xxx 10110100 10110xxx 10111xxx 10111100 10111xxx	D, 8 bit D, 8 bit D, 8 bit D, 8 bit	0-3 5-7 0-3 5-7	0,1,2,3,4,5 0,1,2,3,4,5 0,1,4,5 0,1,4,5	2 to 5 2 to 4 2 to 5 2 to 4	9 to 16 9 to 15 9 to 16 9 to 15
C0-C3 C4 C5-C7 C8-CB CC CD-CF	Move 16 Move Move 16 XOR 16 XOR XOR 16	11000xxx 11000100 11000xxx 11001xxx 11001100 11001xxx	D, 16 bit D, 8 bit D, 16 bit D, 16 bit D, 8 bit D, 8 bit	0-3 4 5-7 0-3 4 5-7	0,1,4,5 0,1,4,5 0,1,4,5 0,1,4,5 0,1,4,5 0,1,4,5	2 to 6 4 2 to 4 2 to 6 4 2 to 4	14 to 22 22 17 to 20 14 to 22 22 17 to 20
D0-D3 D4 D5-D7 D8-DB DC DD-DF	OR 16 OR OR 16 AND 16 AND AND 16	11010xxx 11010100 11010xxx 11011xxx 11011100 11011xxx	D, 16 bit D, 8 bit D, 16 bit D, 16 bit D, 8 bit D, 16 bit	0-3 4 5-7 0-3 4 5-7	0,1,4,5 0,1,4,5 0,1,4,5 0,1,4,5 0,1,4,5 0,1,4,5	2 to 6 4 2 to 4 2 to 6 4 2 to 4	14 to 22 22 17 to 20 14 to 22 22 17 to 20
E0-E3 E4 E5-E7 E8-EB EC ED-EF	Subtract 16 Subtract Subtract 16 Add 16 Add Add 16	11100xxx 11100100 11100xxx 11101xxx 11101100 11101xxx	D, 16 bit D, 8 bit D, 16 bit D, 16 bit D, 8 bit D, 16 bit	0-3 4 5-7 0-3 4 5-7	0,1,2,3,4,5 0,1,2,3,4,5 0,1,2,3,4,5 0,1,2,3,4,5 0,1,2,3,4,5 0,1,2,3,4,5	2 to 6 4 2 to 4 2 to 6 4 2 to 4	14 to 22 22 17 to 20 14 to 22 22 17 to 20

† For the case where the d field is 15, the destination operand is the Stack Pointer.

xxx Any dyadic mode number (0 to 3, 5 to 7). Mode 4 is only use for 8-bit instructions using the corresponding 16-bit instruction opcode.

TABLE 6

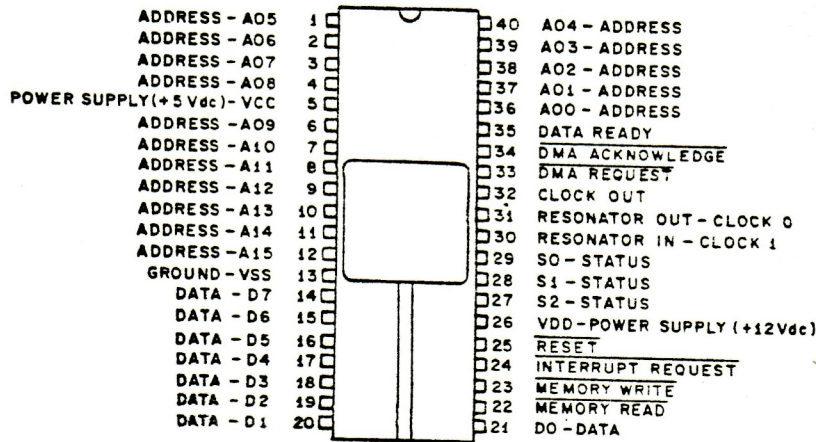
OPCODE ASSIGNMENTS

HEX	FUNCTION	BINARY	TYPE	MODE(S)	COND	BYTES	CYCLES
F0-F3	Compare	11110xxx	D, 16 bit	0-3	0,1,2,3,4,5	2 to 6	14 to 22
F4	Compare	11110100	D, 8 bit	4	0,1,2,3,4,5	4	22
F5-F7	Compare	11110xxx	D, 16 bit	5-7	0,1,2,3,4,5	2 to 4	17 to 20
F8		11111000					
F9		11111001					
FA	Test	11111010	D, 8 bit	4	0,1,4,5	4	22
FB		11111011					
FC		11111100					
FD		11111101					
FE		11111110					
FF	Illegal Opcode	11111111					

xxx Any dyadic mode number (0 to 3, 5 to 7). Mode 4 is only used for 8-bit instructions using the corresponding 16-bit instruction opcode.

TABLE 7

LEAD FUNCTION DIAGRAM



Note
212B -

FIGURE 4

PIN DESCRIPTION

A bar over a pin's functional identifier (e.g. READ) indicates activation by a low TTL logic level (0). Pin numbers are given in parenthesis ().

POWER PINS

- V_{CC} +5 Volt supply. (5)
- V_{DD} +12 Volt supply. (26)
- V_{SS} Ground reference (0 volt). (13)

ADDRESS PINS

- A₀₀ - A₁₅ Address bus. 16 pins used to select a memory location or I/O port. Output 3-state. (36-40, 1-4, 6-12)

DATA PINS

- D₀ - D₇ Data Bus. 8 pins used for memory or I/O data transfer. Input/Output

CLOCK PINS

- CLK 0, CLK 1 External Resonator In/Out. 2 pins used to connect to an external resonator circuit or an external clock signal source. (31,30)

CLK OUT

- Clock Output Signal. TTL compatible signal used to synchronize external devices. Available whether using internal clock and resonator or external clock source. (32)

A clock cycle starts when CLK OUT makes a high to low transition.

PIN DESCRIPTION (Cont'd)

OTHER INPUT PINS

INT REQ Interrupt Request. External device requests interrupt by applying a low on this pin. Request is latched in last cycle of current instruction if interrupt enable condition is set. On granting interrupt, CPU stores CR and PC on stack (RAM), clears interrupt enable, and then reads from hex address FFFF (interrupt acknowledge). **INT REQ** must remain low until after request is acknowledged by the read from hex address FFFF. CPU reads data from data bus and uses lower byte as interrupt handler routine address; upper byte is forced to zero. **INT REQ** should return high before address is permitted to change. (24)

INTERRUPT ADDRESS (HEX)	FUNCTION
FFFF	Interrupt Acknowledge
0000	Reset Handler (Vector)
0000<N<=00FF	Interrupt Handler (Vector)
0008	Illegal Opcode (Trap Vector)

TABLE 8

RESET (Note 1) Reset CPU Low (active) signal; reset request is latched on last cycle of current instruction. Nonmaskable. CPU stores CR and PC on stack (RAM), clears interrupt enable, and sets the PC to zero. After **RESET**, instruction execution starts at hex memory location 0000. **RESET** should return high before address is permitted to change. (25)

DMA REQ DMA Request. Low (active) signal; tells CPU that external device wants access to data and address buses. CPU polls **DMA REQ** at end of each clock cycle. Request is not granted if **DATA READY** lead is low and CPU is in a **READ** or **WRITE** operation. (33)

RELIABILITY

See General Section, Reliability and Handling.

HANDLING PRECAUTIONS

STATIC SENSITIVE DEVICE. See General Section, Reliability and Handling.

DATA READY Signal used to synchronize CPU with slow memory or I/O devices. A high signal indicates that answering device is ready for data transfer on a **READ** or **WRITE** operation; a low signal tells CPU to wait. (35)

OTHER OUTPUT PINS

DMA ACK CPU Generated DMA Acknowledge. Master bus control is passed to requesting device and all address, data, memory read, and memory write pins are put in high-impedance state. (34)

READ Read from Memory. Low (active) signal; remains low until end of **READ** cycle and remains active until a non-**READ** cycle occurs. (22)

WRITE Write Into Memory. Low (active) signal; is delayed from beginning of, and ends before end of **WRITE** cycle. Data valid at mid-cycle. Returns to high state at end of each **WRITE** cycle. (23)

S₀, S₁, S₂ Status. Three pins indicate various internal states of CPU. (29,28,27)

S ₂	S ₁	S ₀	ASSIGNMENT
0	0	0	PC Change
0	0	1	IR Fetch, no CR
0	1	0	RP Change
0	1	1	IR Fetch, with CR
1	0	0	No Reportable Status
1	0	1	Halt
1	1	0	SP Change
1	1	1	Trap or Trouble

TABLE 9

Note 1: In order for **RESET** to reset the CPU, it must access memory (for stack pointer operations) with the **DATA READY** lead at a logic one. Since the SP setting is not known at initial reset, it is necessary to guarantee that **DATA READY** is forced to a logic one.

INPUT AND OUTPUT WAVEFORMS (Note 1,2)

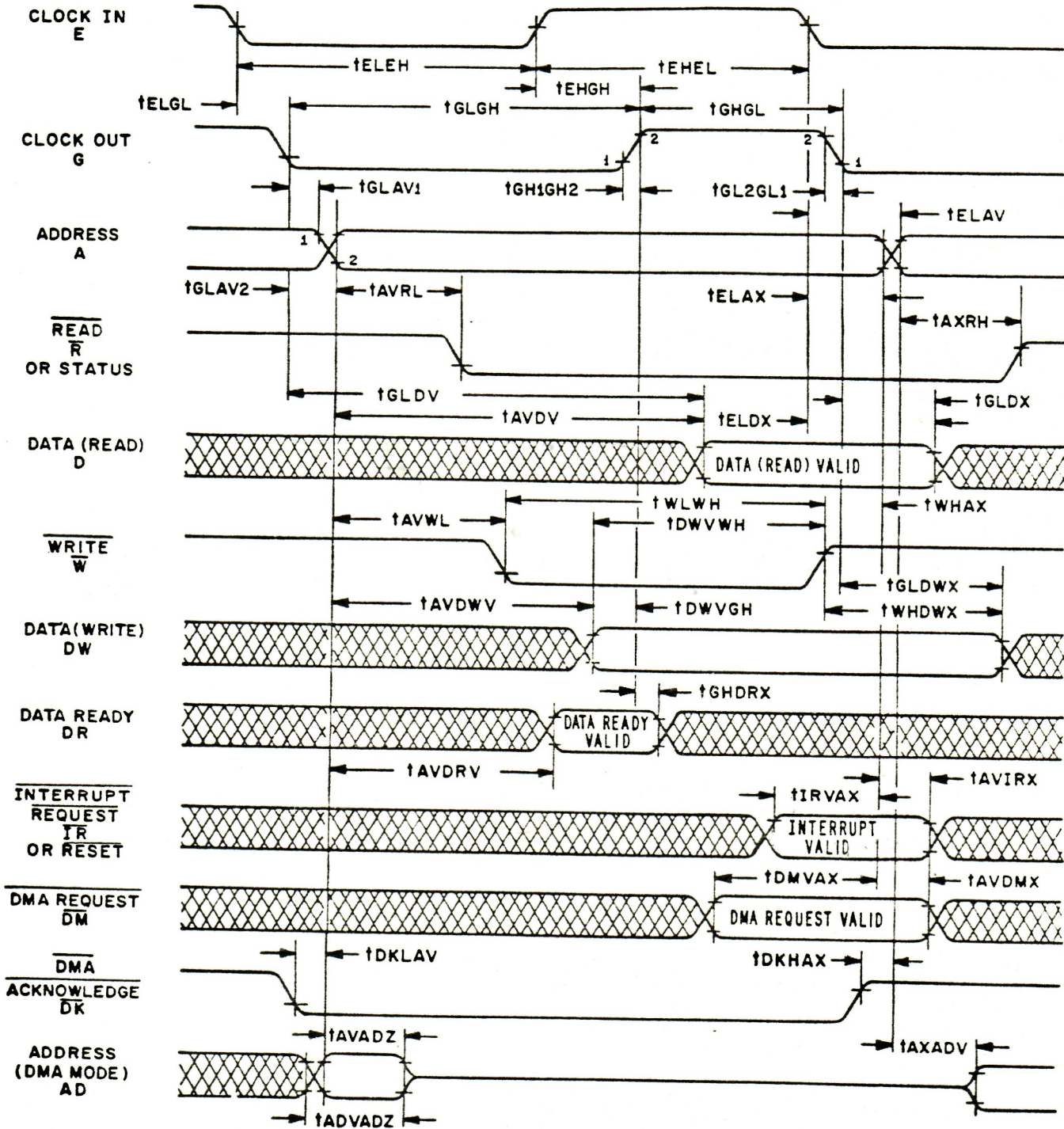


FIGURE 5

Note 1: The values of these parameters for t_{ELAX} , t_{ELAV} , and t_{ELDX} are valid only for the 212D at 85°C. The parameter t_{WLWH} shown is valid only for the 212D, E.

Note 2: t_{ELDX} - Enable Low to Data Valid
 t_{GLDX} - Output Low to Data Valid

TIMING CHARACTERISTICS

This table is for the 212B of series 7 or greater, the 212C of series 9 or greater, and all 212D and E versions.

DESCRIPTION		OBSOLETE SYMBOLS	SYMBOLS	MIN	MAX	UNITS
Clock In Pulse Width—Low	212B	T_{in}	tELEH	243	—	ns
	212C	T_{in}	tELEH	270	—	ns
	212D	T_{in}	tELEH	225	—	ns
	212E	T_{in}	tELEH	166	—	ns
Clock In Pulse Width—High	212B	T'_{in}	tEHEL	243	—	ns
	212C	T'_{in}	tEHEL	270	—	ns
	212D	T'_{in}	tEHEL	225	—	ns
	212E	T'_{in}	tEHEL	166	—	ns
Clock Out Pulse Width—Low	212B,C,D	T_{out}	tGLGH	tELEH + 10	tELEH + 80 or tELEH + tEHEL-400 ^①	ns
	212E	T_{out}	tGLGH	tELEH	tELEH + 60 or tELEH + tEHEL-400 ^①	ns
Clock Out Pulse Width—High	212B,C,D	T'_{out}	tGHGL	tEHEL-80 or 400 ^②	tEHEL-10 or 3000 ^②	ns
	212E	T'_{out}	tGHGL	tEHEL-60 or 400 ^②	tEHEL or 3000 ^②	ns
Clock In to Clock Out Delay Time—Low	212B,C,D	T_{c1}	tELGL	—	120	ns
	212E	T_{c1}	tELGL	—	100	ns
Clock In to Clock Out Delay Time—High	212B,C,D	T_{c2}	tEHGH	—	180	ns
	212E	T_{c2}	tEHGH	—	160	ns
Clock Out to Address Transmission Time—Low	212B,C,D,E	T_{ac}	tGLAV1	0	45	ns
Clock Out to Address Valid	212B,D	T'_{ac}	tGLAV2	15	60	ns
	212C	T'_{ac}	tGLAV2	10	60	ns
	212E	T'_{ac}	tGLAV2	0	60	ns
Change of Read (or Status) Delay Time	212B,C,D,E	T_{crd}	tAVRL	- 10	20	ns
Change of Read (or Status) Delay Time	212B,C,D,E	T'_{crd}	tAXRH	- 15	20	ns
Data (Read) Access Time— Off Chip Memory	212B,D	T_{access}	tAVDV	tELEH + tEHEL-120	—	ns
	212C,E	T_{access}	tAVDV	tELEH + tEHEL-100	—	ns
Clock Out Access Time	212B,C,D	T_{clkacc}	tGLDV	tELEH + tEHEL-70	—	ns
	212E	T_{clkacc}	tGLDV	tELEH + tEHEL-50	—	ns

①—Whichever is greater.

②—Whichever is less.

TIMING CHARACTERISTICS (Cont'd)

This table is for the 212B of series 7 or greater, the 212C of series 9 or greater, and all 212D and E versions.

DESCRIPTION		OBSOLETE SYMBOLS	SYMBOLS	MIN	MAX	UNITS
Data (Read) Hold Time	212B,C,D,E	T_{cdh}	tGLDX	0	—	ns
Memory Write Start Delay Time	212B,D,E	T_{cw}	tAVWL	50	200	ns
Memory Write End Delay Time	212C*	T_{cw}	tAVWL	75	200	ns
	212B,C,D,E	T_{wc}	tWHAX	5	80	ns
Memory Write Pulse Width	212B,C,D,E	T_{wp}	tWLWH	tELEH + tEHEL-253	—	ns
Available Data (Write) to Memory Write Time	212B,C,D,E	T_{wd}	tDWVWH	tELEH + tEHEL-190	—	ns
Data (Write) Valid to Clock Out Time-High	212B,C,D,E	T_{wdh}	tDWVGH	0	—	ns
Data (Write) Out Delay Time	212B,C,D,E	T_{wds}	tAVDWV	—	120	ns
Data (Write) Hold Time	212B,C,D,E	T_{wdw}	tWHDWX	15	—	ns
Data Hold Time After Clock Out	212B,D,E	T_{wdc}	tGLDWX	10	—	ns
Data Ready Access Time	212B,C,D	T_{mracc}	tAVDRV	tELEH-100	—	ns
	212E	T_{mracc}	tAVDRV	tELEH-76	—	ns
Data Ready Hold Time	212B,C,D,E	T_{ryh}	tGHDRX	0	—	ns
Interrupt or Reset Setup Time	212B,C,D,E	T_{is}	tIRVAX	80 ⁷⁷	—	ns
Interrupt or Reset Hold Time	212B,C,D,E	T_{ih}	tAVIRX	100 ⁹⁷	—	ns
DMA Request Setup Time	212B,C,D,E	T_{dmas}	tDMVAX	100	—	ns
DMA Request Hold Time	212B,C,D,E	T_{dmah}	tAVDMX	0	—	ns
DMA Acknowledge On Delay Time	212B,C,D,E	T_{dmak}	tDKLAV	-50	70	ns
DMA Acknowledge Off Delay Time	212B,C,D,E	T_{dmax}	tDKHAX	-50	70	ns
Address (DMA Mode) Off Delay Time	212B,C,D,E	T_{dma}	tAVADZ	—	100	ns
Address (DMA Mode) Float Delay Time	212B,C,D,E	T_{dmaa}	tADVADZ	0	—	ns
Address (DMA Mode) On Delay Time	212B,C,D,E	T_{dma}	tAXADV	—	100	ns
Clock Out Rise Time	212B,C,D,E	T_r	tGH1GH2	—	1.0	ns/pF
Clock Out Fall Time		T_f	tGL2GL1	—	1.0	ns/pF
Data Latch After Clock In (Note 1)		T_{dl}	tELDX	35	68	ns
Address Hold Time After Clock In (Note 1)		T_{ah}	tELAX	80	—	ns
Clock In To Address Valid (Note 1)		T_{aci}	tELAV	—	160	ns

* MIN value is for series 13 and above. Below series 13, MIN value is the same as 212D.

Note 1: The values of these parameters for tELAX, tELAV, and tELDX are valid only for the 212D at 85°C.
tELDX—Enable Low to Data Valid.

TIMING CHARACTERISTICS—REFERENCE ONLY

This table is for the Manufacture Discontinued 212B of series 6 or less, and the 212C of series 8 or less.

DESCRIPTION			OBSOLETE SYMBOLS	SYMBOLS	MIN	MAX	UNITS
Clock In Pulse Width	Low	212B	T_{in}	tELEH	243	—	ns
		212C	T_{in}	tELEH	270	—	ns
	High	212B	T'_{in}	tEHEL	243	—	ns
212C		T'_{in}	tEHEL	270	—	ns	
Clock Out Pulse Width	Low	212B,C	T_{out}	tGLGH	tELEH + 10	tELEH + 110 or tELEH + tEHEL - 400 ^①	ns
	High		T'_{out}	tGHGL	tEHEL - 110 or 400	tEHEL - 10 or 300 ^①	ns
Clock In to Clock Out Delay Time—	Low		T_{c1}	tELGL	—	230	ns
	High		T_{c2}	tEHGH	—	290	ns
Clock Out To Address Transition Time—Low			T_{ac}	tGLAV1	0	—	ns
Clock Out To Address Valid			T'_{ac}	tGLAV2	0	60	ns
Change of Read (or Status) Delay Time			T_{crd}	tAVRL	—	85	ns
			T'_{crd}	tAXRH	—	85	ns
Data (Read) Access Time— Off Chip Memory		212B,C	T_{access}	tAVDV	tELEH + tEHEL - 150	—	ns
Clock Out Access Time		212B	T_{clkacc}	tGLDV	tELEH + tEHEL - 120	—	ns
		212C	T_{clkacc}	tGLDV	—	—	—
Data (Read) Hold Time		212B,C	T_{dh}	tGLDX	0	—	ns
Memory Write Delay Time	Start	212B,C	T_{cw}	tAVWL	50	220	ns
	End		T_{wc}	tWHAX	5	125	ns
Memory Write Pulse Width			T_{wp}	tWLWH	tELEH + tEHEL - 290	—	ns
Available Data (Write) to Memory Write Time			T_{wd}	tDWVWH	tELEH + tEHEL - 290	—	ns
Data Write Valid To Clock Out Time—High Data (Write) Out Delay Time Data (Write) Hold Time			T_{wdh}	tDWVGH	0	—	ns
			T_{wds}	tAVDWV	—	235	ns
			T_{wdw}	tWHDWX	15	—	ns
Data Ready Access Time Data Ready Hold Time			T_{mracc}	tAVDRV	tELEH - 100	—	ns
		T_{ryh}	tGHDRX	0	—	ns	

①—Whichever is greater.

TIMING CHARACTERISTICS—REFERENCE ONLY (Con't)

This table is for the Manufacture Discontinued 212B of series 6 or less, and the 212C of series 8 or less.

DESCRIPTION		OBSOLETE SYMBOLS	SYMBOLS	MIN	MAX	UNITS	
Interrupt or Reset Time	Set up	212B,C	T _{is}	tIRVAX	80	—	ns
	Hold		T _{ih}	tAVIRX	200	—	ns
DMA Request Time	Set up		T _{dmas}	tDMVAX	200	—	ns
	Hold		T _{dmah}	tAVDMX	0	—	ns
DMA Acknowledge Delay Time	On		T _{dmak}	tDKLAV	-110	100	ns
	Off		T _{dmax}	tDKHAX	-110	100	ns
Address (DMA Mode) Delay Time	Off		T _{dma}	tAVADZ	—	160	ns
	Float		T _{dmaa}	tADVADZ	0	—	ns
	On		T' _{dma}	tAXADV	—	160	ns
Clock Out	Rise Time		T _r	tGH1GH2	—	1.0	ns/pF
	Fall Time	T _f	tGL2GL1	—	1.0	ns/pF	

ELECTRICAL CHARACTERISTICS

		APPLIED LIFE LIMITS†		
		MIN	MAX	UNITS
Output Sink Current (V _O = 0.4 Vdc) (V _O = 0.5 Vdc)	IOL	1.6	—	mAdc
	IOL	2.0	—	mAdc
Output Source Current <i>2.7 → V_O</i> (V _O = 3.2 Vdc)	IOH	300 160	<i>212C</i> —	<i>μ</i> mAdc
Leakage Current (V _I or V _O = 5.25 Vdc) (V _I or V _O = 0)	IL	-400	400	nAdc
	IL	-400	400	nAdc
Supply Currents (f = 0Hz, ALU on) (f = 0Hz, ALU off) *(f = 2.06 MHz, VDD = 12.6 Vdc) 212B *(f = 1.85 MHz, VDD = 12.6 Vdc) 212C *(f = 2.22 MHz, VDD = 12.6 Vdc) 212D *(f = 3.0 MHz, VDD = 12.6 Vdc) 212E V _{cc}	IDD	—	10	mAdc
	IDD	—	5.0	mAdc
	IDD	—	45	mAdc
	IDD	—	42	mAdc
	IDD	—	48	mAdc
	IDD	—	61	mAdc
	ICC	—	5.0	mAdc
Input Voltages High Level Low Level	V _{IH}	1.8	V _{cc} + .25	Vdc
	V _{IL}	-0.25	0.8	Vdc

†Applied Life Limits are intended as guides for the circuit and systems designer since they take into consideration possible device variation throughout life.

*The maximum I_{dd} at other frequencies can be calculated using the following: I_{dd} = 10 + 17 × FREQ (MHz) mA

OPERATING CONDITIONS

		MIN	NOM	MAX.	UNITS
Supply Voltages (TTL Circuits)	VDD	11.4	12.0	12.6	Vdc
	VSS	0	0	0	Vdc
	VCC	4.75	5.0	5.25	Vdc
Input Capacitance	CI	—	10	—	pF
Output Capacitance	CL	—	25	—	pF
Operating Temperature	TA	-40		85	°C

OUTLINE (#102)

