in nanoBGA2

Datasheet

Revision 1.80

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VIA TECHNOLOGIES, INC.

Designed by CenTaur technology *in Texas*

This is **Version 1.80** of the VIA C7 Processor Datasheet.

LIFE SUPPORT POLICY

VIA processor products are not authorized for use as components in life support or other medical devices or systems (hereinafter life support devices) unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of VIA.

1. **Life support devices are devices which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.**
2. **This policy covers any component of a life support device or system whose failure to perform can cause the failure of the life support device or system, or to affect its safety or effectiveness.**

Revision History

Document Release	Date	Revision	Initials
1.0	07/14/05	Initial Release	CJH
1.01	07/14/05	Updated Table 2-3 Removed C7-M reference on page 17	CJH
1.6	12/25/05	Updated Brand detection, Timing Diagrams, Power Consumption	CJH
1.70	01/18/06	Updated AC Timing descriptions	CJH
1.80	02/09/06	Added non-PowerSaver capable C7	CJH

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1

INTRODUCTION

The VIA C7 processor is based on a unique internal architecture and is manufactured using IBM's advanced 90nm SOI CMOS technology. This architecture and process technology provide a highly compatible, high-performance, and low-power consumption solution for most computing markets.

When considered individually, the compatibility, function, performance, cost, and power dissipation of the VIA C7 processor family are all very competitive. When considered as a whole, the VIA C7 processor family offers a breakthrough level of *value*.

The intent of this datasheet is to make it easy for a direct user—a board designer, a system designer, or a BIOS developer—to use the VIA C7 processor.

Section 1 of the datasheet summarizes the key features of the VIA C7 processor. Section 2 specifies the primary programming interface, Section 3 does the same for the bus interface. Sections 4, 5, and 6 specify the classical datasheet topics of AC timings, ballouts, and mechanical specifications.

Section 7 documents the VIA C7 processor machine specific registers (MSRs).

1.1 BASIC FEATURES

With its very low power dissipation, the VIA C7 processor is ideally suited for most applications. All versions share the following common features (except as noted):

- Extremely low power consumption
- PowerSaver provides fastest performance state switching
  - **VIA C7's support only two performance states. Except the VIA C7 1.5 GHz 25W does not support PowerSaver.**
- World's fastest AES encryption using the Advanced Cryptography Engine (ACE)
- Secure Hash Algorithm: SHA-1 and SHA-256
- Montgomery Multiplier

- Random Number Generator
- Thermal Monitor 1, Thermal Monitor 2, and Catastrophic Thermal Protection
- Multi-processor support: Dual processing (SMP).
- MMX, SSE, SSE2, and SSE3-compatible instructions
- Two large (64-KB each, 4-way) Level 1 caches
- 128-KB Level 2 victim cache (32-way)
- L2 Hardware Prefetch
- Two large TLBs (128 entries each, 8-way)
- Branch Target Address Cache with 1k entries each identifying 2 branches
- Unique and sophisticated branch prediction mechanisms
- Bus speeds up to 800 MHz
- Software-compatible with thousands of x86 software applications available
- Very small die-30 mm^2 in IBM 90nm SOI technology
- nanoBGA2 package 21mm x 21mm (400 balls)

1.2 PROCESSOR VERSIONS

Typically, there are five specification parameters that characterize different versions of a processor family: package, voltage, maximum case temperature, external bus speed, and internal MHz.

The VIA C7 processor family is available in small form factor package, nanoBGA2, just 21mm x 21mm. The minimum and maximum processor core voltages are configured at the factory. After powerup, PowerSaver can dynamically adjust the processor core voltage can select between those pre-configured values.

The internal operating frequency (MHz) of a particular VIA C7 processor is defined by two parameters: the specified external bus speed and the core clock-to-bus ratio. VIA C7 processors operate the bus up to 800 MHz (200 MHz BCLK). The minimum and maximum core clock-to-bus ratios are also configured at the factory. PowerSaver allows the dynamic adjustment of the processor's core clock-to-bus ratio between the two factory configured minimum and maximum ratios.

This datasheet provides the specification for these VIA C7 processors:

- 2.0 GHz
- 1.8 GHz
- 1.6 GHz
- 1.5 GHz
- 1.5 GHz (25W, without PowerSaver)
- 1.3 GHz
- 1.0 GHz

Future versions of the VIA C7 processor may provide other speed grades, bus speed combinations and different core voltages.

More information on these topics is included in Sections 4, 5, and 6 of this datasheet.

1.3 COMPATIBILITY

VIA C7 processors are the epitome of compatibility. To verify compatibility of the VIA C7 processor with real PC applications and hardware, VIA has performed extensive testing of boards and peripherals, thousands of software applications, and over forty operating systems. Currently, BIOS support for the VIA C7 processor is available from Award, AMI, Phoenix, General Software, and Insyde.

The VIA C7 processor supports SSE, SSE2, and SSE3 instructions for better video, audio, and faster 3D graphics. Other functions are provided and are identified to software with the CPUID instruction. The VIA C7 processor carefully follows the protocol for defining the availability of these optional features. Both the additional and omitted optional features are covered in more detail in Section 2 of this datasheet.

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SECTION

2

PROGRAMMING INTERFACE

2.1 GENERAL

The VIA C7 processor's functions include:

- All basic x86 instructions, registers, and functions
- All floating-point (numeric processor) instructions, registers and functions
- All basic operating modes: real mode, protect mode, virtual-8086 mode
- System Management Interrupt (SMI) and the associated System Management Mode (SMM)
- All interrupt and exception functions
- All debug functions (including the new I/O breakpoint function)
- All input/output functions
- All tasking functions (TSS, task switch, etc.)
- Processor initialization behavior
- Page Global Enable feature
- MMX™ instructions
- SSE, SSE2, and SSE3 instructions
- PAT (Page Attribute Table)
- VME (Virtual Mode Enhancements)
- SYSENTER/SYSEXIT functions

However, there are some software differences between the VIA C7 processor and the Intel Pentium-M processor. These differences fall into three groups:

- **Implementation-specific differences**. Examples are cache and TLB testing features, and performance monitoring features that expose the internal implementation features. These types of functions are incompatible among *all* different x86 implementations.
- **Omitted functions**. Some processor functions are not provided on the VIA C7 processor because they are not used or are not needed in the targeted PC systems. Examples are some specific bus functions such as functional redundancy checking and performance monitoring. Other examples are architectural extensions such as support for 36 bit addressing.

  These types of differences are similar to those among various versions of the processors. The CPUID instruction is used by system software to determine whether these features are supported.
- **Low-level behavioral differences**. A few low-level VIA C7 processor functions are different from Intel Pentium-M because the results are (1) documented in the documentation as *undefined*, and (2) known to be different for different x86 implementations. That is, compatibility with the Intel Pentium-M processor for these functions is clearly not needed for software compatibility (or they would not be different across implementations).
- **Additional Functions**. VIA C7 processors provide enhanced features such as cryptography.

2.2 ADDITIONAL FUNCTIONS

The VIA C7 processor includes a suite of security technologies called Padlock.

Advanced Cryptography Engine: ACE

Padlock's Advanced Cryptography Engine provides the world's fastest AES encryption implementation. Wherever AES software encryption implementations are used today, it can be optimized for ACE with minimal effort. World class AES performance is a user-level instruction away as only one opcode handles encrypt and decrypt functions. See the Padlock programming guide for further details.

Random Number Generator: RNG

VIA C7 processors incorporate two random number generators on the processors die for a fast source of entropy. See the Padlock programming guide for further details.

Secure Hash Algorithm: SHA-1 and SHA-256

VIA C7 processors have a hardware implementation of the secure hash standard algorithm, SHA-1 and SHA-256 (FIPS 180-1). SHA is used to compute a condensed representation of text, useful in many cryptography applications. See the Padlock programming guide for further details.

Montgomery Multiplier

VIA C7 processors include a Montgomery Multiplier for fast modular exponentiation. Modular exponentiation is commonly used in public key cryptography. See the Padlock programming guide for further details.

NoExecute: NX

The VIA C7 processor provides data execution protection support used in Microsoft Windows XP SP2.

Multi-processor:

The VIA C7 processor provides dual processing (SMP) support. Multi-processing requires specific chip-set support.

2.3 MACHINE-SPECIFIC FUNCTIONS

2.3.1 GENERAL

All x86 processor implementations provide a variety of *machine-specific functions*. Examples are cache and TLB testing features and performance monitoring features that expose the internal implementation features.

This section describes the VIA C7 processor machine-specific functions that are most likely used by software, and compares them to related processors where applicable. Section 7 describes these machine-specific registers (*MSRs*).

This section covers those features of x86 processors that are used to commonly identify and control processor features. All x86 processors have the same mechanisms, but the bit-specific data values often differ.

2.3.2 STANDARD CPUID INSTRUCTION FUNCTIONS

The CPUID instruction is available on all contemporary x86 processors. The CPUID instruction has two standard functions requested via the EAX register. The first function returns a vendor identification string in registers EBX, ECX, and EDX. The second CPUID function returns an assortment of bits in EAX and EDX that identify the chip version and describe the specific features available. See the following table.

Table 2-1. CPUID Return Values (EAX = 0)

EAX	TITLE	OUTPUT
0	Largest Function Input Value	EAX=1 EBX:EDX:ECX =”CentaurHauls”
1	Processor Signature and Feature Flags	EAX[3:0]=Stepping ID EAX[7:4]=Model ID EAX[11:8]=Family ID EAX[13:12]=Type ID EBX=Reserved ECX=Additional Feature Flags (see Table 2-3) EDX=Feature Flags (see Table 2-2)

The specific feature flag details in EDX when EAX == 1 are listed in Table 2-2. Additional feature flag details in ECX are listed in

Table 2-2. CPUID Feature Flag Values (EAX = 1)

EDX bit	Name	Function	C7	Notes
0	FPU	The processor provides an on-die x87 floating-point unit.	1	
1	VME	Virtual Mode Extensions are available.	1	
2	DE	Debugging Extensions are available.	1	
3	PSE	The processor supports 4 MB pages.	1	
4	TSC	Time Stamp Counter available.	1	
5	MSR	Machine Specific Registers are available.	1	
6	PAE	Physical Address Extensions	1	
7	Reserved	Not supported.	0	
8	CX8	CMPXCHG8B instruction available.	1	1
9	APIC	Processor contains internal APIC.	1	
10	Reserved	Not supported.	0	
11	SEP	Fast system calls are available using SYSENTER/SYSEXIT instructions.	1	
12	MTRR	Memory Type Range Registers are available.	1	
13	PGE	Global paging is available.	1	
14	Reserved	Not supported.	0	
15	CMOV	CMOV and FCMOV instructions available.	1	
16	PAT	Page Attribute Table available.	1	
17	Reserved	Not Supported.	0	
18	Reserved	Not Supported.	0	
19	CLFSH	CLFLUSH instruction supported.	1	
20	Reserved	Not Supported.	0	
21	Reserved	Not Supported.	0	
22	ACPI	Thermal Monitor and other thermal controls	1	
23	MMX™	MMX™ instructions are available.	1	
24	FXSR	Fast Floating-Point Save and Restore instructions available.	1	
25	SSE	SSE instructions are available.	1	
26	SSE2	SSE2 instructions are available.	1	
27	Reserved	Not Supported.	0	
28	Reserved	Not Supported.	0	
29	TM	Thermal monitor is supported	1	
30	Reserved	Not Supported.	0	
31	PBE	Pending-Break Enable is supported	1	

Notes On CPUID Feature Flags:

1. The CMPXCHG8B instruction is provided and always enabled, however, it can be disabled in the corresponding CPUID function bit 8 to avoid a bug in an early version of Windows NT. However, this default can be changed via bit 1 in the FCR MSR.

Table 2-3. Additional CPUID Feature Flag Values (EAX = 1)

ECX bit	Name	Function	C7
0	SSE3	SSE3 instructions available.	1
6:1	Reserved	Not supported.	0
7	EPS	PowerSaver / Enhanced Power-Saver available.	1
8	TM2	Thermal Monitor 2 available.	1
31:9	Reserved	Not supported.	0

2.3.3 EXTENDED CPUID INSTRUCTION FUNCTIONS

The VIA C7 processor supports extended CPUID functions. These functions provide additional information about the VIA C7 processor. Extended CPUID functions are requested by executing CPUID with EAX set to any value in the range 0x80000000 through 0x80000006.

The following table summarizes the extended CPUID functions.

Table 2-4. Extended CPUID Functions

EAX	TITLE	OUTPUT
80000000	Largest Extended Function Input Value	EAX=80000006 EBX,ECX, EDX[20]= NX support if set
80000001	Processor Signature and Feature Flags	EAX=Processor Signature EBX,ECX=Reserved EDX=Extended Feature Flags
80000002	Processor Name String	EAX,EBX,ECX,EDX
80000003	Processor Name String	EAX,EBX,ECX,EDX
80000004	Processor Name String	EAX,EBX,ECX,EDX
80000005	TLB and L1 Cache Information	EAX = Reserved EBX = TLB Information ECX = L1 Data Cache Information EDX = L1 Instruction Cache Information
80000006	L2 Cache Information	EAX, EBX, EDX = Reserved ECX = L2 Cache Information

Largest Extended Function Input Value (EAX==0x80000000)

Returns 0x80000006 in EAX, the largest extended function input value.

Processor Signature and Feature Flags (EAX==0x80000001)

Returns processor version information in EAX and Extended CPUID feature flags in EDX. EDX bit 20 indicates NoExecute support. NoExecute is used in Windows XP SP2 for virus protection.

Processor Name String (EAX==0x80000002–0x80000004)

Returns the name of the processor, suitable for BIOS to display on the screen (ASCII). The string can be up to 48 characters in length. For the VIA C7, the processor name string indicates the processor core and maximum operating frequency in ASCII. The string " VIA Esther processor XXXX MHz" is returned by extended function EAX = 0x80000002 through EAX=0x80000004 as follows:

Table 2-5. Processor Name String

CPUID call	EAX	EBX	ECX	EDX
0x80000002	0x20202020	0x20202020	0x20202020	0x20202020
0x80000003	0x56202020	0x45204149	0x65687473	0x72702072
0x80000004	0x7365636F	0x20726F73	0x30303031	0x007A484D

L1 Cache Information (EAX == 0x80000005)

Returns information about the implementation of the TLBs and caches:

Table 2-6. L1 Cache & TLB Configuration Encoding

REGISTER	DESCRIPTION	VALUE
EAX	Reserved	
EBX	TLB Information	
EBX[31:24]	D-TLB associativity	8
EBX[23:16]	D-TLB # entries	128
EBX[15: 8]	I-TLB associativity	8
EBX[7: 0]	I-TLB # entries	128
ECX	L1 Data Cache Information	
ECX[31:24]	Size (Kbytes)	64
ECX[23:16]	Associativity	4
ECX[15: 8]	Lines per Tag	1
ECX[7: 0]	Line Size (bytes)	64
EDX	L1 Instruction Cache Information	
EDX[31:24]	Size (Kbytes)	64
EDX[23:16]	Associativity	4
EDX[15: 8]	Lines per Tag	1
EDX[7: 0]	Line Size (bytes)	64

L2 Cache Information (EAX == 0x80000006)

Returns information about the implementation of the L2 cache:

Table 2-7. L2 Cache Configuration Encoding

REGISTER	DESCRIPTION	VALUE
EAX, EBX, EDX	Reserved	
ECX	L2 Data Cache Information	
ECX[31:16]	Size (Kbytes)	128
ECX[15:12]	Associativity	32
ECX[11: 8]	Lines per Tag	1
ECX[7: 0]	Line Size (bytes)	64

2.3.4 CENTAUR EXTENDED CPUID INSTRUCTION FUNCTIONS

The VIA C7 processor supports special CPUID functions. These functions provide additional information about the VIA C7 processor. Centaur CPUID functions are requested by executing CPUID with EAX set to 0xC0000000, 0xC0000001, or 0xC0000002.

Table 2-8. Centaur Extended CPUID Instruction Functions

EAX Input	Title	Output
0xC0000000	Largest Centaur Extended Function Input Value	EAX=0xC0000001
0xC0000001	Centaur Extended Feature Flags	EDX=Centaur Extended Feature Flags EAX,EBX,ECX=Reserved
0xC0000002	Centaur CPUID Performance Data	See Table 2-10

Table 2-9. Centaur Extended CPUID Feature Flag Values

EDX bit	Centaur CPUID Extended Feature Flags	VIA C7
0	Reserved	0
1	Reserved	0
2	Random Number Generator (RNG) Present	1
3	Random Number Generator (RNG) Enabled	1
4	Reserved	0
5	Reserved	0
6	Advanced Cryptography Engine (ACE) Present[1]	1
7	Advanced Cryptography Engine (ACE) Enabled	1
8	ACE2 present[1]	1
9	ACE2 enabled	1
10	Padlock Hash Engine present[1]	1
11	Padlock Hash Engine enabled	1
12	Padlock Montgomery Multiplier present[1]	1
13	Padlock Montgomery Multiplier enabled	1

Table 2-10. Centaur Extended CPUID Performance Data

Reg	Bit	Description	Default
EAX		**Current Temperature in Celsius**	
	7:0	Fractional temp	0/1
	31:8	Current Temperature in Celsius	0/1
EBX		**Mirror of Misc_Performance_Status MSR 0x198[31:0]**	
	7:0	Current Voltage (16*[7:0] + 700)mV	0/1
	15:8	Current clock multiplier in hexadecimal. e.g. 6X is 00110b. 16X is 10000b	0/1
	23:16	Reserved	0/1
	31:24	Lowest clock ratio	0/1
ECX		**Mirror of Misc_Performance_Status MSR 0x198[63:32]**	
	7:0	Highest Voltage encoding (16*[7:0] + 700)mV	0/1
	15:8	Highest clock ratio	0/1
	23:16	Lowest Voltage encoding	0/1
	31:24	Lowest clock ratio	0/1
EDX		**Mirror of EBL_CR_POWERON MSR 0x2A**	
	14	1 MB Reset Vector 0: 0xFFFFFFF 1: 0x000FFFF0	0
	17:16	APIC Cluster ID	0
	19:18	Input Front Side Bus clock 00: 100 MHz 01: 133 MHz 10: 200 MHz 11: 166 MHz	0
	21:20	APIC Agent ID	0
	26:22	Current clock ratio in hexadecimal. e.g. 6X is 00110b. 16X is 10000b	0/1
	31:27	Reserved	0/1

2.3.5 PROCESSOR IDENTIFICATION

The VIA C7 processor provides several machine-specific features. These features are identified by the standard CPUID function EAX=1. Other machine-specific features are controlled by MSRs. Some of these features are not backward-compatible with the predecessors in the VIA processor family.

System software must not assume that all future processors in the VIA processor family will implement all of the same machine-specific features, or even that these features will be implemented in a backward-compatible manner. In order to determine if the processor supports particular machine-specific features, system software should follow the following procedure.

Identify the processor as a member of the VIA processor family by checking for a Vendor Identification String of "CentaurHauls" using CPUID with EAX=0. Once this has been verified, system software must determine the processor version in order to properly configure the machine-specific registers.

The CPUID family 6 model A core of the VIA C7 is shared with other VIA processors. To identify these brand variants, use the MSR instruction to read register 1153h and use the Exclusive OR (XOR) function between bit fields 21:20 and 19:18.

Table 2-11. VIA Processor Brand Detection

VIA BRAND	MSR 1153h [21:20] XOR MSR 1153h [19:18]
Reserved	11b
VIA C7-M	00b
VIA C7	01b
VIA Eden	10b

NOTE: Valid only for CPUID Family 6 Model A.

In general system software can determine the processor version by comparing the Family and Model Identification fields returned by the CPUID standard, extended, or Centaur extended functions.

If the processor version is not recognized then system software must not attempt to activate any machine-specific feature.

2.3.6 EDX VALUE AFTER RESET.

After reset the EDX register holds a component identification number as follows:

EDX[31:4]	EDX[13:12]	EDX[11:8]	EDX[7:4]	EDX[3:0]
Reserved	Type ID	Family ID	Model ID	Stepping ID

The specific values for the VIA C7 processor are listed here:

PROCESSOR	TYPE ID	FAMILY ID	MODEL ID	STEPPING ID
VIA C7	0	6	10	Begins at 9

2.3.7 CONTROL REGISTER 4 (CR4)

Control register 4 (CR4) controls some of the advanced features of x86 processors. The VIA C7 processor provides a CR4 with the following specifics:

Table 2-12. CR4 Bits

CR4 BITS - MEANING	VIA C7	PENTIUM-M	NOTES
0: VME: Enables VME feature	0/1	0/1	
1: PVI: Enables PVI feature	0/1	0/1	
2: TSD: Makes RDTSC inst privileged	0/1	0/1	
3: DE: Enables I/O breakpoints	0/1	0/1	
4: PSE: Enables 4-MB pages	0/1	0/1	
5: PAE: Enables address extensions	r	r	
6: MCE: Enables machine check exception	0/1	0/1	1
7: PGE: Enables global page feature	0/1	0/1	
8: PCE: Enables RDPMC for all levels	0/1	0/1	
9: OSFXSR: Enables FXSAVE//FXRSTOR Support	0/1	r	
10: OSXMMEXCPT: O/S Unmasked Exception Support	0/1	r	
31:11 – reserved	r	r	

Notes On CR4

General: a "0/1" means that the default setting of this bit is 0 but the bit can be set to (1). A "0" means that the bit is always 0; it cannot be set. An "r" means that this bit is reserved. It appears as a 0 when read, and a GP exception is signaled if an attempt is made to write a 1 to this bit.

1. The VIA C7 processor Machine Check has different specifics than the Machine Check function of other x86 processors.

2.3.8 MACHINE-SPECIFIC REGISTERS

The VIA C7 processor implements the concept of Machine Specific Registers (MSRs). RDMSR and WRMSR instructions are provided and the CPUID instruction identifies that the processor supports MSRs.

In general, the MSRs have no usefulness to application or operating system software and are not used. (This is to be expected since the MSRs are different on each processor.) Section 7 contains a detailed description of the VIA C7 processor's MSRs.

2.4 OMITTED FUNCTIONS

This section summarizes those functions that are not in the VIA C7 processor. A bit in the CPUID feature flags indicates whether these feature are present or not.

Page Size Extensions: PSE-36

This function is omitted since the target operating systems for the VIA C7 do not require greater than 4 GB of system memory.

Other Functions

Model specific registers pertaining to Machine Check, and Debug, Performance Monitoring, and Trace features are not supported.

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SECTION

3

HARDWARE INTERFACE

3.1 BUS INTERFACE

The majority of the balls within the bus interface are involved with the physical memory and I/O interface. The remaining balls are power and ground balls, test and debug support balls, and various ancillary control functions. The balls and associated functions are listed and described in this section.

Core-to-Bus Frequency Ratio Control

The VIA C7 processor supports both fixed and software control of the core-to-bus frequency ratio. At reset, the processor boots to the factory configured minimum ratio. System BIOS uses PowerSaver to set the operating frequency to the highest supported ratio. System software adjusts the operating frequency using PowerSaver performance states for the desired balance of power consumption and performance.

Bus Frequency Selection

The VIA C7 processor bus frequency is provided by the motherboard through motherboard strapping options. The VIA C7 processor is designed to operate at bus clock frequencies of 100, 133,166, or 200 MHz.

3.1.1 CLARIFICATIONS

Power Supply Voltage

The voltage provided to the processor core is accomplished through the processors VID balls.

The VIA C7 processor expects a voltage mapping corresponding to a VRM using the voltage range indicated in Table 3-1.

Table 3-1. Core Voltage Settings

VID[5:0]	V_{CC}	VID[5:0]	V_{CC}	VID[5:0]	V_{CC}	VID[5:0]	V_{CC}
000000	**1.708**	010000	**1.452**	100000	**1.196**	110000	**0.940**
000001	**1.692**	010001	**1.436**	100001	**1.180**	110001	**0.924**
000010	**1.676**	010010	**1.420**	100010	**1.164**	110010	**0.908**
000011	**1.660**	010011	**1.404**	100011	**1.148**	110011	**0.892**
000100	**1.644**	010100	**1.388**	100100	**1.132**	110100	**0.876**
000101	**1.628**	010101	**1.372**	100101	**1.116**	110101	**0.860**
000110	**1.612**	010110	**1.356**	100110	**1.100**	110110	**0.844**
000111	**1.596**	010111	**1.340**	100111	**1.084**	110111	**0.828**
001000	**1.580**	011000	**1.324**	101000	**1.068**	111000	**0.812**
001001	**1.564**	011001	**1.308**	101001	**1.052**	111001	**0.796**
001010	**1.548**	011010	**1.292**	101010	**1.036**	111010	**0.780**
001011	**1.532**	011011	**1.276**	101011	**1.020**	111011	**0.764**
001100	**1.516**	011100	**1.260**	101100	**1.004**	111100	**0.748**
001101	**1.500**	011101	**1.244**	101101	**0.988**	111101	**0.732**
001110	**1.484**	011110	**1.228**	101110	**0.972**	111110	**0.716**
001111	**1.468**	011111	**1.212**	101111	**0.956**	111111	**0.700**

RESET#
The VIA C7 processor is reset by the assertion of the RESET# ball.

Thermal Diode
An on-die thermal diode supports thermal monitoring via the THERMDN and THERMDP balls.

Thermal Monitor
The VIA C7 processor provides a second on-die thermal sensor for advanced thermal control. See Section 6.6.

Advanced Peripheral Interrupt Controller (APIC)
APIC is supported by the VIA C7 processor.

3.1.2 OMISSIONS

Breakpoint and Performance Monitoring Signals
The VIA C7 processor internally supports instruction and data breakpoints. However, the processor does not support the external indication of breakpoint matches. Similarly, the VIA C7 processor contains performance monitoring hooks internally, but it does not support the indication of performance monitoring events.

Error Checking
The VIA C7 processor does not support error checking. There are no BERR#, BINIT#, AERR#, AP#[1:0], DEP#[7:0], IERR#, RP#, and RSP# balls.

3.2 BALL DESCRIPTION

Table 3-2. Ball Descriptions

Ball Name	Description	I/O
A[18:3]# A30#	The VIA C7 has 36 address signals multiplexed on a 20-bit source-synchronous bus. The address phase is composed of 4 phases within a single BCLK.	I/O
A20M#	A20 Mask causes the CPU to make (force to 0) the A20 address bit when driving the external address bus or performing an internal cache access. A20M# is provided to emulate the 1 MByte address wrap-around that occurs on the 8086. Snoop addressing is not affected.	I
ADS#	Address Strobe begins a memory/I/O cycle and indicates the address bus and transaction request signals are valid.	I/O
ADSTBN0# ADSTBP0#	Address Strobes for A[30,18:3]# and REQ[2:0]# ADSTBN0 are negative-edge going data strobes used to latch A[30]#,A[18:3]# on odd data beat transfers. ADSTBP0]# are negative-edge going data strobes used to latch A[30]# & A[18:3]# on even data beat transfers. External termination is unnecessary.	I/O
BCLK0 BCLK1	Bus Clock provides the fundamental timing for the VIA C7 CPU. The frequency of the VIA C7 CPU input clock determines the operating frequency of the CPU's bus. External timing is referenced to the crossing point of the rising edge of BCLK0 and the falling edge of BCLK1	I
BEVO[3:0]	BEVO[3:0] are hardware strapping option balls that allow additional functionality and testability. BEV0[3:0] signals are supplemental and not necessary for regular operation. To assist VIA in debugging, these are testing status balls that could be brought out to test connector. BEVO3 must be connected to ground for normal operation.	I/O
BNR#	Block Next Request signals a bus stall by a bus agent unable to accept new transactions.	I/O
BPRI#	Priority Agent Bus Request arbitrates for ownership of the system bus.	I
BREQ[3:0]#	BREQ[3:0]# signals request access to the system bus. In uniprocessor designs , BREQ[3:1]# are considered “No Connects” and BREQ0# requires 220 ohm pullup to Vccp	I/O
BSEL[1:0]	Currently unused. Leave unconnected or route to test point.	O
CF[8:0]	CF[8:0] should be connected to ground with zero Ohm resistors. These resistors are strapping options that are determined by the platform BOM. Routing is not critical	II
COMP[0] COMP[2]	The COMP signals require 27.4 Ohm precision termination. The COMP resistors need to placed within 200mils of the processor.	I
D[63:0]#	Data Bus signals are bi-directional signals which provide the data path between the VIA C7 CPU and external memory and I/O devices. The data bus must assert DRDY# to indicate valid data transfer. These are also 4X signals and are driven 4 times a clock period. The falling edge of DSTBP[3:0]# and DSTBN[3:0]# will latch D[63:0]#. D[63:0]# are divided into signal groups with a corresponding DSTBN#/DSTBP# pair along with a DINV# for polarity. Hence: D[15:0]# are grouped with DSTBN[0], DSTBP[0], and DINV[0]#. D[31:16]# are grouped with DSTBN[1], DSTBP[1], and DINV[1]#. D[47:32]# are grouped with DSTBN[2], DSTBP[2], and DINV[2]#. D[63:48]# are grouped with DSTBN[3], DSTBP[3], and DINV[3]#.	I/O
DBSY#	Data Bus Busy is asserted by the data bus driver to indicate data bus is in use.	I/O

Ball Name	Description	I/O
DEFER#	Defer is asserted by target agent (e.g., north bridge) and indicates the transaction cannot be guaranteed as an in-order completion.	I
DINV[3:0]#	DINV[3:0] reflect the polarity of D[63:0]#. They are active if the data bus values are inverted. The source driving agent will invert the data bus signals if more than half the bits in the data bus signal group change in the next bus cycle. DINV[0]# governs the polarity of D[15:0]# DINV[1]# governs the polarity of D[31:16]# DINV[2]# governs the polarity of D[47:32]# DINV[3]# governs the polarity of D[63:48]#	I/O
DP[3:0]#	DP[3:0]# provide parity for the data signals D[63:0]#. Connect these to the north bridge if supported. If parity is not used, then leave unconnected or route to test point.	I
DPSLP#	DPSLP#, when asserted in the stop grant or sleep state, will transition the processor into the deep sleep state. The system should then remove BCLK[1:0]# to arrive at the deep sleep state. Reviving the clocks and then deasserting DPSLP# will transition the processor back to the sleep state	I
DPWR#	Asserted by the north bridge to indicate that a data return cycle is pending.	I
DRDY#	Data Ready is asserted by data driver to indicate that a valid signal is on the data bus.	I/O
DSTBN[3:0]#	DSTBN[3:0]# are negative-edge going data strobes used to latch D[63:0]# on odd data beat transfers. DSTBN[0]# latch D[15:0]# and DINV[0]# DSTBN[1]# latch D[31:16]# and DINV[1]# DSTBN[2]# latch D[47:32]# and DINV[2]# DSTBN[3]# latch D[63:48]# and DINV[3]#	I/O
DSTBP[3:0]#	DSTBP[3:0]# are negative-edge going data strobes used to latch D[63:0]# on even data beat transfers. DSTBP[0]# latch D[15:0]# and DINV[0]# DSTBP[1]# latch D[31:16]# and DINV[1]# DSTBP[2]# latch D[47:32]# and DINV[2]# DSTBP[3]# latch D[63:48]# and DINV[3]#	I/O
FERR#	FPU Error Status indicates an unmasked floating-point error has occurred. FERR# is asserted during execution of the FPU instruction that caused the error.	O
HIT#	Snoop Hit indicates that the current cache inquiry address has been found in the cache (exclusive or shared states).	I/O
HITM#	Snoop Hit Modified indicates that the current cache inquiry address has been found in the cache and dirty data exists in the cache line (modified state).	I/O
IGNNE#	Ignore Numeric Error forces the VIA C7 CPU to ignore any pending unmasked FPU errors and allows continued execution of floating point instructions.	I
INIT#	Assertion resets integer registers and does not affect internal cache or floating point registers. INIT# active during RESET# will execute BIST (Built-In Self-Test).	I
INTR	Indicates external interrupt. Becomes LINT0 when using the APIC.	I
LOCK#	Lock Status is used by the CPU to signal to the target that the operation is atomic.	I/O
MPI	MPI controls termination for multi-processor configurations. For uni-processors designs, MPI should tied to ground or pulled to ground with a zero ohm resistor for testability. Placement is not critical	I
NMI	Indicates Non-Maskable Interrupt. Becomes LINT1 when using the APIC.	I
PROCHOT#	PROCHOT# is an output from the on-die thermal sensor whose assertion indicates the processor has reached its maximum operating temperature. When PROCHOT# is active, the processor will activate its thermal protection circuitry.	O
PSI#	PSI# is asserted when the processor enters the deep sleep state. This is a signal to the system VRM to transition to the deeper sleep state.	O
PWRGD	Indicates that the processor's VCC is stable. Care should be taken to ensure this signal has no glitches or noise.	I
REQ[2:0]#	Request Command is asserted by bus driver to define current transaction type. REQ[2:0] are part of the address group.	I/O
RESET#	Resets the processor and invalidates internal cache without writing back.	I
RS[2:0]#	Response Status signals the completion status of the current transaction when the CPU is the response agent.	I
RSVD	Reserved for future use.	-
SLP#	Sleep, when asserted in the stop grant state, causes the CPU to enter the sleep state.	I

Ball Name	Description	I/O
SMI#	System Management (SMM) Interrupt forces the processor to save the CPU state to the top of SMM memory and to begin execution of the SMI services routine at the beginning of the defined SMM memory space. An SMI is a high-priority interrupt than NMI.	I
STPCLK#	Stop Clock causes the CPU to enter the stop grant state.	I
TCK	Clock Input for the JTAG port.	I
TDI	Data Input for the JTAG port.	I
TDO	Data Output for the JTAG port.	O
THERMDN THERMDP	The anode/cathode pair of an on-chip thermal diode for measuring the processor core temperature.	O
THERMTRIP#	THERMTRIP# is asserted when the processor exceeds the absolute maximum die temperature. When asserted, the processor will transition to the lowest performance state and cease execution. System platform can use THERMTRIP# to power down the entire system for catastrophic thermal protection.	O
TMS	Test Mode Select for the JTAG port	I
TRDY#	Target Ready indicates that the target is ready to receive a write or write-back transfer from the CPU.	I
TRST#	Test Reset for the JTAG port.	I
V_{CC}	Core voltage power supply.	I
V_{CCA}[2:0]	Isolated power supply for the internal PLL's. VCCA0 provides power to the on-die thermal monitor.	I
V_{CCP}	Processor bus termination voltage power supply.	I
V_{CC_SENSE}	Isolated low impedance trace to processor core power for use in power measurement or VRM feedback.	O
VID[5:0]	The Voltage Identification signals indicate the core voltage required from the platform VRM.	O
V_{SS}	Ground power supply.	-
V_{SS_SENSE}	Isolated low impedance ground trace to processor core for use in power measurement or VRM feedback.	O

3.3 POWER MANAGEMENT

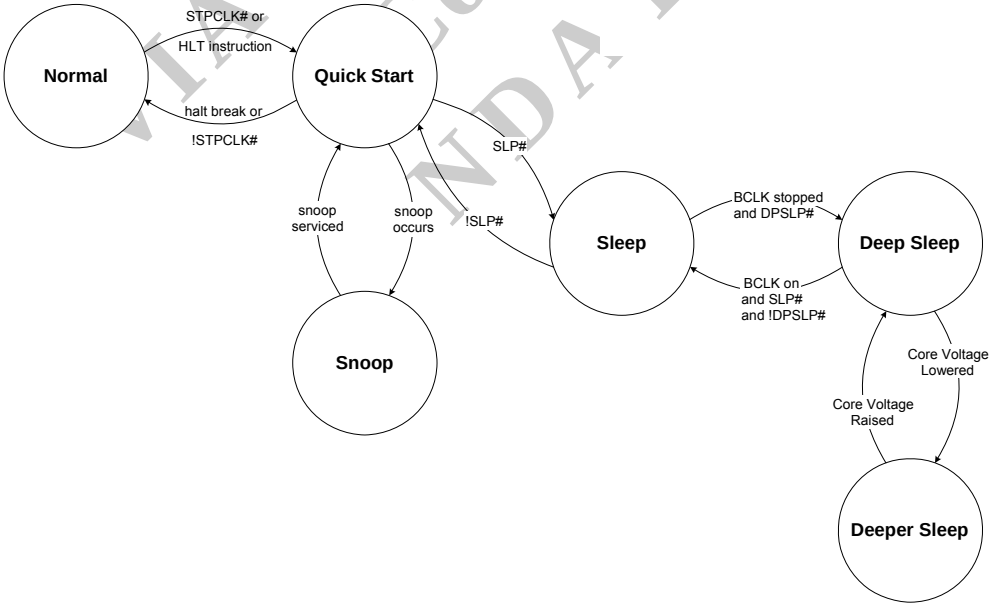
The VIA C7 processor provides both static and dynamic power management.

The VIA C7 processor supports five power management states: NORMAL, QUICKSTART, SLEEP, DEEP SLEEP, and DEEPER SLEEP state.

The VIA C7 processor uses dynamic power management techniques to reduce power consumption in the NORMAL state. In NORMAL state, the on-chip arrays, selected datapaths, and the associated control logic are powered down when not in use. Also, units that are in use attempt to minimize switching of inactive nodes.

- NORMAL state is the normal operating state for the processor.
- QUICKSTART state is the low power state where most of the processor clocks do not toggle. It is entered when the STPCLK# signal is asserted or when the processor executes the HALT instruction. Snoop cycles are supported in this state.
- SLEEP state is the low power state where only the processor's PLL (phase lock loop) toggles. It is entered from STOP GRANT state when the processor samples the SLP# signal asserted. Snoop cycles that occur while in SLEEP state or during a transition into or out of SLEEP state will cause unpredictable behavior.
- DEEP SLEEP state is a very low power state. It is entered when the BCLK signal is stopped while the processor is in the SLEEP state. Snoop cycles are completely ignored in this state. The processor will drive PSI# upon the entry of the Deep Sleep.
- DEEPER SLEEP state is the lowest power state. It is entered when the processor core voltage is lowered while the processor is in the DEEP SLEEP state. Snoop cycles are completely ignored in this state.

Figure 3-1. Power Management State Diagram



3.4 POWERSAVER

PowerSaver is a highly advanced power management mechanism for the VIA C7 processor. PowerSaver technology allows the dynamic adjustment of the operating frequency and operating voltage. The VIA C7 can only change from the highest supported performance state to the lowest supported performance state: intermediate performance states are not guaranteed to work and are not officially supported. System software can use PowerSaver to request the sufficient amount of performance. Each individual performance state (P-State) is described in the system bios according to 8.4.4 of the ACPI 3.0 specification.

The VIA C7 processor incorporates two on-chip core clock PLL's. This allows the processor to ping-pong between two frequencies instantaneously. In the simplest scenario, where there are only two clock frequencies of interest and no voltage changes, the transition can be instantaneous with no latency. In more complex scenarios, where there are multiple clock frequencies of interest, the "old" frequency can continue to be used while the new frequency is ramped up. The transition is still instantaneous from a software point of view (code still executes), but there is a latency associated with switching to the ramping "new" frequency.

VIA C7 allows for a clean hardware approach to processor operating point transitions. The transitions are performed instantaneously from a software and functional point of view. Snoops and interrupts, for example, are unaffected by transitions.

See the BIOS Writer's guide for further details.

3.5 JTAG

The VIA C7 processor has a JTAG scan interface that is used for test functions. Boundary scan is available through the JTAG interface.

SECTION

4

ELECTRICAL SPECIFICATIONS

4.1 DC SPECIFICATIONS

4.1.1 RECOMMENDED OPERATING CONDITIONS

Functional operation of the VIA C7 processor is guaranteed if the conditions in Table 4-1 are met. Sustained operation outside of the recommended operating conditions may damage the device.

Table 4-1. Recommended Operating Conditions

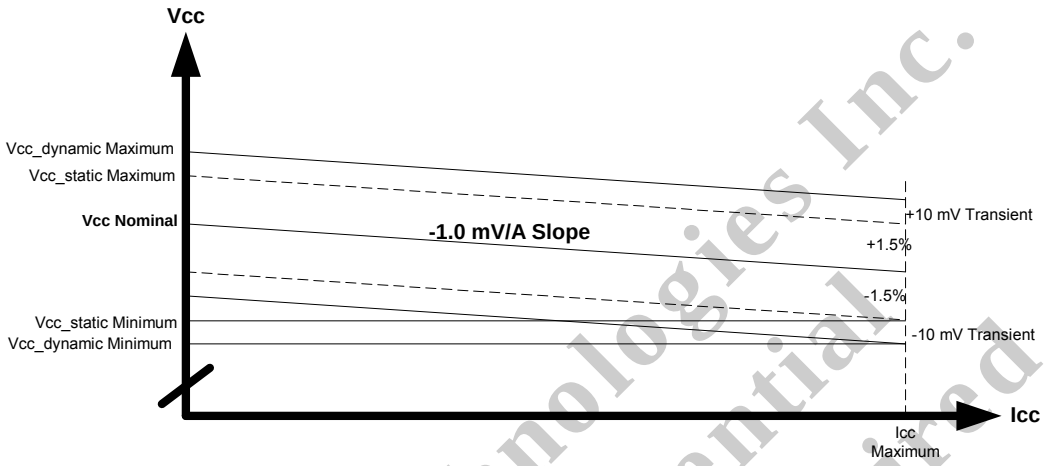
PARAMETER	MIN	NOM	MAX	UNITS	NOTES
Operating Junction Temperature	0		100	°C	
V_{CC} Voltage		1.148 1.084 1.004 0.956	1.148	V	2
V_{CC} Static Tolerance	Use LoadLine figure below			V	1
V_{CC} Dynamic Tolerance				V	
$V_{CC,BOOT}$ Boot Voltage		1.200		V	2
V_{CCP} Termination Voltage	0.997	1.05	1.102	V	
$V_{CCDPRSLP}$ Deeper Sleep Voltage		0.748		V	
I_{CC}		15	25	A	
I_{DPRSLP} Deeper Sleep Current			0.66	A	
V_{CCA} PLL supply voltage	-5%	1.8 or 1.5	+5%	V	

PARAMETER	MIN	NOM	MAX	UNITS	NOTES
I_{CCA} PLL supply current		10	130	mA	3

Notes:

1. DC measurement. Regulator Circuit should support current draw up to 25A.
2. Vcc 1.148V is maximum sustained voltage. Vcc_boot is a temporary power-up voltage for initialization.
3. Measured at 1.8V Vccp.

Figure 4-1.Vcc Loadline



4.1.2 MAXIMUM RATINGS

While functional operation is not guaranteed beyond the operating ranges listed in Table 4-1, the device may be subjected to the limits specified in Table 4-2 without causing long-term damage.

These conditions must not be imposed on the device for a sustained period—any such sustained imposition may damage the device. Likewise exposure to conditions in excess of the maximum ratings may damage the device.

Table 4-2. Maximum Ratings

PARAMETER	MIN	MAX	UNITS	NOTES
Storage Temperature	-40	150	°C	
Supply Voltage (V_{CC})	-0.5	1.20	V	
I/O Voltage	-0.5	V_{CCP} +0.5	V	

4.1.3 DC CHARACTERISTICS

Table 4-3. System Bus BCLK Characteristics

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_L – Input Low Voltage		0		V	
V_H – Input High Voltage	0.660	0.710	0.850	V	
V_{CROSS} – Crossing Voltage	0.25	0.35	0.55	V	
ΔV_{CROSS} – Range of Crossing Voltage			0.140	V	
V_{TH} – Threshold Region	V_{CROSS}-0.100		V_{CROSS}+0.100	V	
I_{LI} – Input Leakage Current			± 15	µA	
C_{PAD}– Pad Capacitance	1.8	2.3	2.75	pF	

Table 4-4. AGTL+ Signal Group DC Characteristics

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
VCCP – I/O & Termination Voltage	0.997	1.05	1.102	V	
GTLREF- Reference Voltage	2/3 VCCP – 2%	2/3 VCCP	2/3 VCCP + 2%	V	2
V_{IH} – Input High Voltage	GTLREF+0.1		VCCP+0.1	V	
V_{IL} – Input Low Voltage	-0.1		GTLREF-0.1	V	
V_{OH} – High Level Output Voltage		VCCP			
R_{TT} – Termination Resistance	47	55	63	Ω	
R_{ON} – Buffer On Resistance	17.7	24.7	32.9	Ω	
I_{LI} – Input Leakage Current			± 100	µA	
C_{PAD}– Pad Capacitance	1.8	2.3	2.75	pF	

Notes:

1. Leakage current is specified for the range between VSS and VCC. GTL I/O's are diode clamped to the VCC and VSS rails.
2. GTLREF is internally generated for VIA C7.

Table 4-5. CMOS DC Characteristics

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
VCCP – I/O & Termination Voltage	0.997	1.05	1.102	V	
V_{IL} -- Input Low Voltage CMOS	-0.1		0.3*VCCP	V	
V_{IH} – Input High Voltage	0.7*VCCP		VCCP+0.1	V	
V_{OL} – Low Level Output Voltage	-0.1	0	0.1*VCCP	V	
V_{OH} – High Level Output Voltage	0.9*VCCP	VCCP	VCCP+0.1	V	
I_{LI} – Input Leakage Current			±100	µA	
C_{PAD}– Pad Capacitance	1.0	2.3	3.0	pF	

Notes:

1. Leakage current is specified for the range between VSS and VCC.
2. I/O's are diode clamped to the VCCP and VSS rails.

Table 4-6. Open Drain Signal Group DC Characteristics

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{PULL} – Maximum Pullup Voltage		VCCP		V	
V_{OL} – Low Level Output Voltage	0	0	0.20	V	
I_{OL} – Low Level Output Current			12	mA	
I_{LI} – Input Leakage Current			±100	µA	
C_{PAD}– Pad Capacitance	1.7	2.3	3.0	pF	

4.2 AC TIMING TABLES AND WAVEFORMS

Figure 4-2. BCLK Generic Clock Timing Waveform

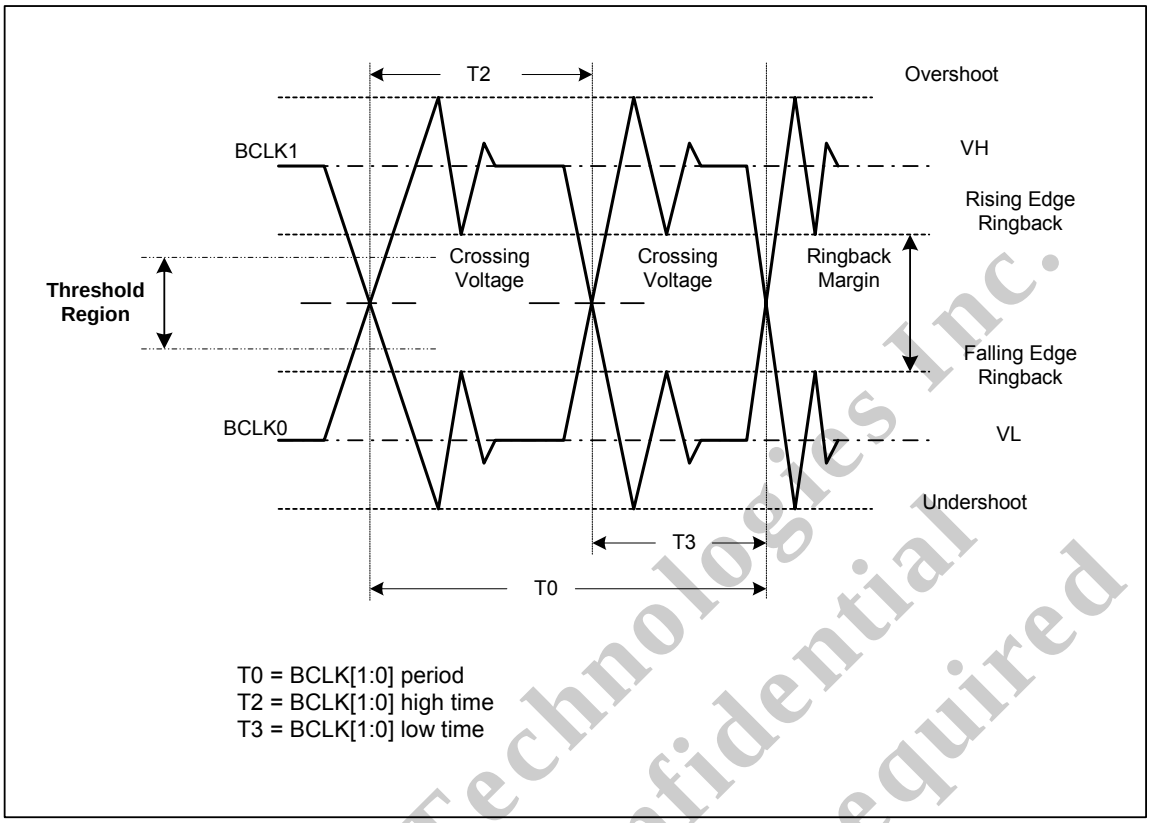


Table 4-7. System Bus Clock AC Specifications (400 MHz)

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT	FIGURE	NOTES[1]
	System Bus Frequency	99.47	100	100.04	MHz	2	
T0	BCLK Period	10		10.2	ns	2	1
T1	BCLK Stability			200	ps	2	2
T2	BCLK High Time	3.94	5	6.12	ns	2	
T3	BCLK Low Time	3.94	5	6.12	ns	2	
T4	BCLK Rise Time	175		700	ps	2	3
T5	BCLK Fall Time	175		700	ps	2	3

Table 4-8. System Bus Clock AC Specifications (533 MHz)

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT	FIGURE	NOTES[1]
	System Bus Frequency	132.62	133.33	133.37	MHz	2	
T0	BCLK Period	7.49		7.54	ns	2	1
T1	BCLK Stability			175	ps	2	2
T2	BCLK High Time	3.0	3.75	4.54	ns	2	
T3	BCLK Low Time	3.94	3.75	4.54	ns	2	
T4	BCLK Rise Time	175		700	ps	2	3
T5	BCLK Fall Time	175		700	ps	2	3

Table 4-9. System Bus Clock AC Specifications (667 MHz)

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT	FIGURE	NOTES[1]
	System Bus Frequency	165.78	166.66	166.72	MHz	2	
T0	BCLK Period	5.998		6.032	ns	2	1
T1	BCLK Stability			175	ps	2	2
T2	BCLK High Time	2.4	3.00	3.632	ns	2	
T3	BCLK Low Time	2.4	3.00	4.632	ns	2	
T4	BCLK Rise Time	175		700	ps	2	3
T5	BCLK Fall Time	175		700	ps	2	3

Notes:

1. The period is the average period and may vary as defined by the period stability specification (T1).
2. Period stability is the maximum timing difference between adjacent BCLK periods.
3. Slew rate is measured between the 35% and 65% points of the BCLK swing (V_L to V_H)

Figure 4-3. FSB Common Clock Valid Delay Timings

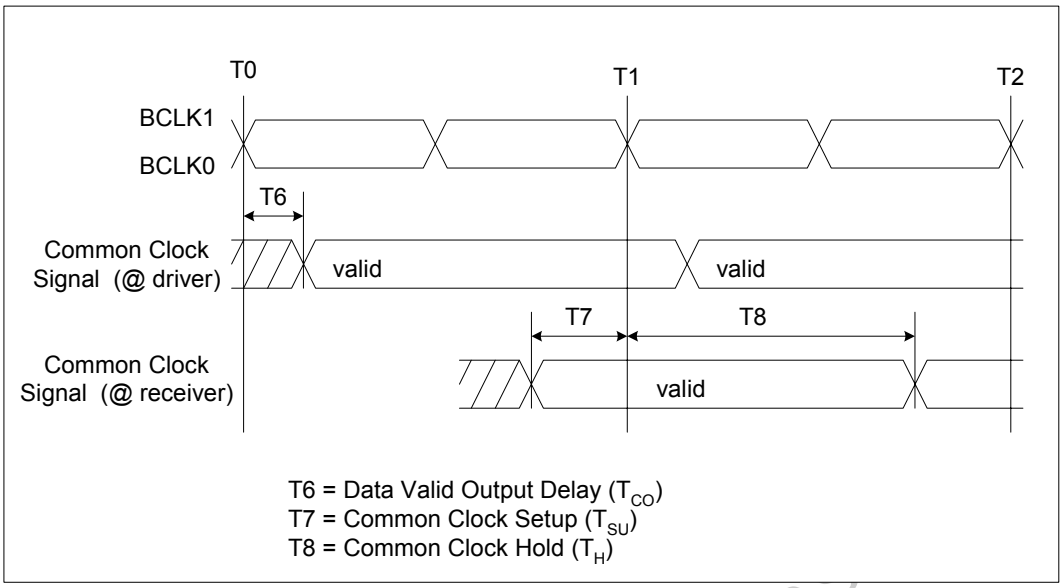


Figure 4-4. FSB Test Circuit

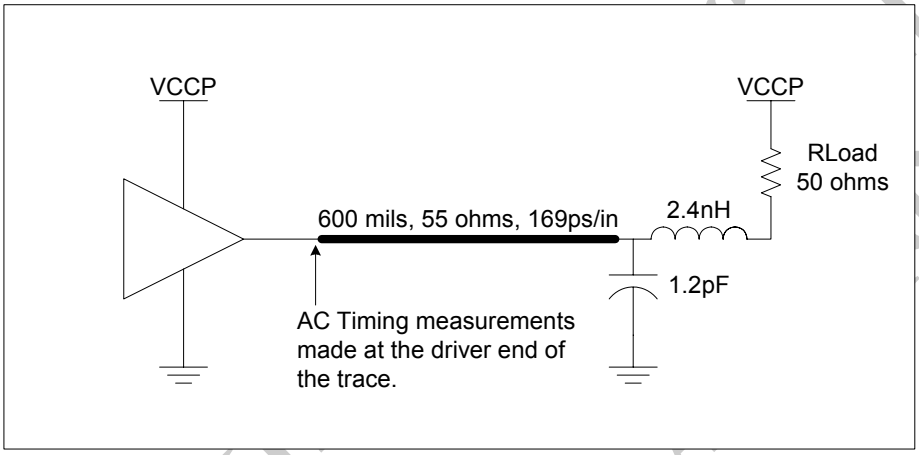


Table 4-10. Common Clock AC Specifications (400 MHz)

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT	FIGURE	NOTES[1,2]
T6	Common Clock Output Valid Delay	0.15		3.3	ns	3	3
T7	Common Clock Input Setup Time	2.9			ns	3	4
T8	Common Clock Input Hold Time	0.4			ns	3	4

Table 4-11. Common Clock AC Specifications (533 MHz)

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT	FIGURE	NOTES[1,2]
T6	Common Clock Output Valid Delay	0.22		2.10	ns	3	3
T7	Common Clock Input Setup Time	2.00			ns	3	4
T8	Common Clock Input Hold Time	0.15			ns	3	4

Table 4-12. Common Clock AC Specifications (667 MHz)

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT	FIGURE	NOTES[1,2]
T6	Common Clock Output Valid Delay	0.22		1.50	ns	3	3
T7	Common Clock Input Setup Time	0.90			ns	3	4
T8	Common Clock Input Hold Time	0.15			ns	3	4

Notes:

1. Guaranteed by design and not 100% tested.
2. All common clock AC timing are referenced to the crossing voltage (Vcross) of BCLK[1:0] at the rising edge of BCLK0. All Common clock input signal timings are referenced at 2/3 VCCP at the processor pad.
3. Valid delay timings for these signals are specified into the test circuit described in Figure 4-4 at 2/3 VCCP.
4. Timing measured at 2/3 VCCP assuming a slew rate between 0.3 V/ns to 4.0 V/ns.

Figure 4-5. Source Synchronous 4X Address Timings (CPU Source)

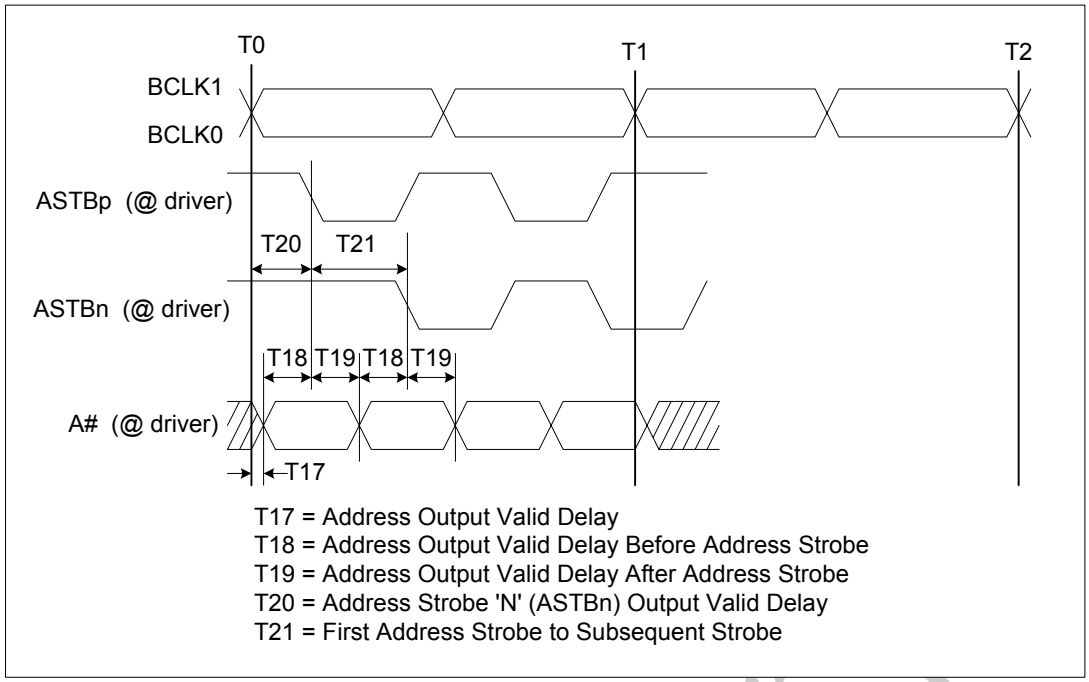


Figure 4-6. Source Synchronous 4X Address Timings (CPU Target)

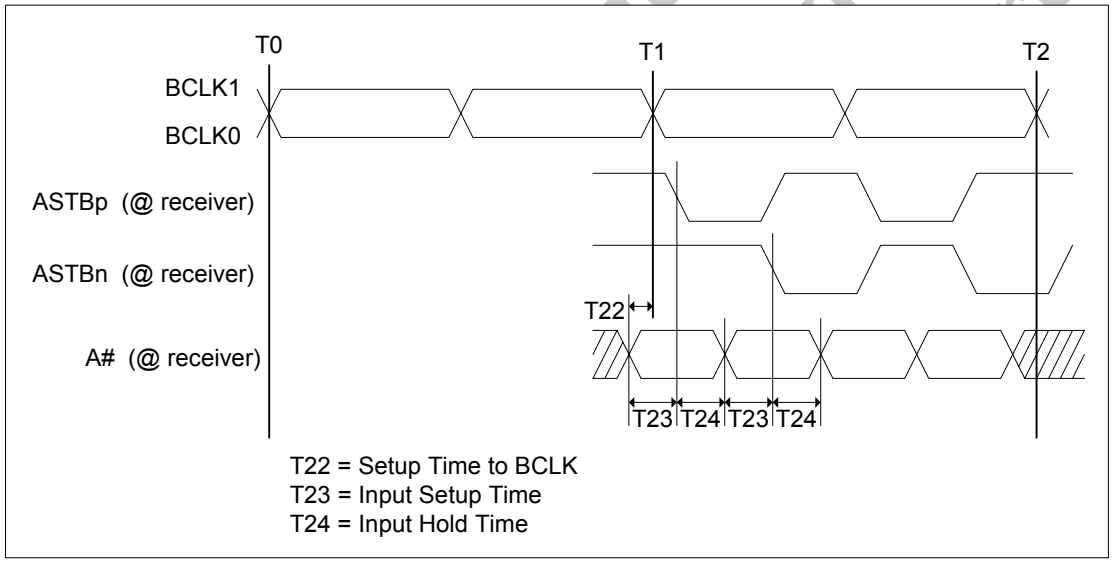
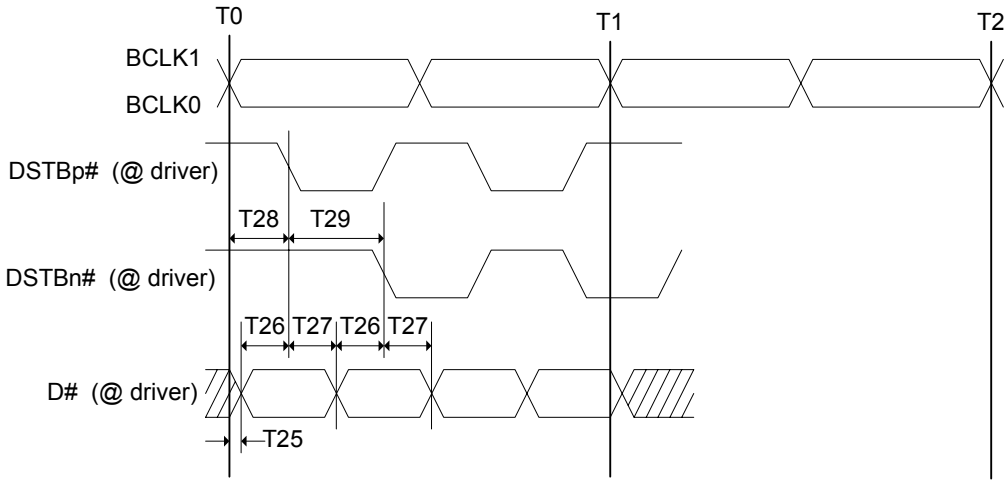
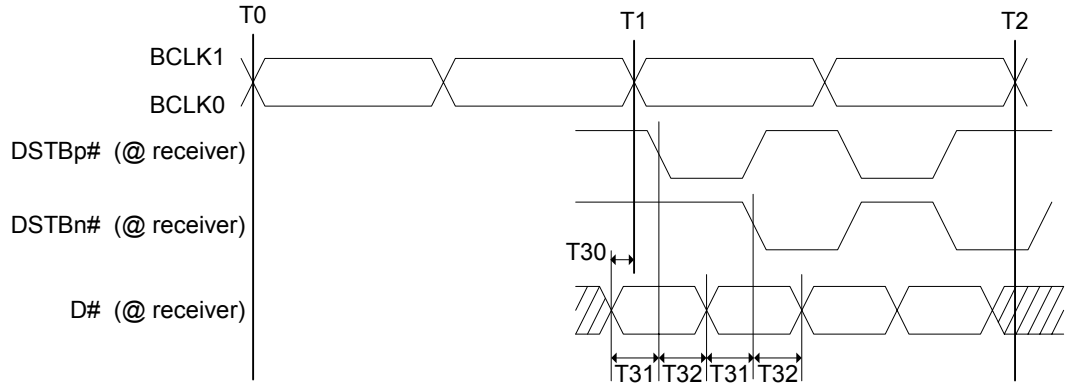


Figure 4-7. Source Synchronous 4X Data Timings (CPU Source)



T25 = Data Output Valid Delay
T26 = Data Output Valid Delay Before Data Strobe
T27 = Data Output Valid Delay After Data Strobe
T28 = Data Strobe 'n' (DSTBP#) Output Valid Delay
T29 = First Data Strobe to Subsequent Strobe

Figure 4-8. Source Synchronous 4X Data Timings (CPU Target)



T30 = Setup Time to BCLK
T31 = Input Setup Time
T32 = Input Hold Time

Table 4-13. 400 MHz FSB Source Synchronous AC Specifications

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT	FIGURE	NOTES[1,2]
T17	Address Output Delay (first address only)	0.0		2.30	ns	6	3
T18	Address Output Valid Before Strobe	0.72			ns	6	3,5
T19	Address Output Valid After Strobe	0.72			ns	6	3,5
T20	Data Strobe 'N' (ASTBP#) Output Valid Delay	1.25		3.55	ns	6	8
T21	First Address Strobe to Subsequent Strobe			2.5	ns	6	
T22	Address Input Setup Time to BCLK	.63			ns	7	7,9
T23	Address Input Setup Time to Strobe	0.34			ns	7	4
T24	Address Input Hold Time to Strobe	0.34			ns	7	4
T25	Data Output Delay (first data only)	0.0		2.30	ns	8	3
T26	Data Output Valid Before Strobe	0.72			ns	8	3,5
T27	Data Output Valid After Strobe	0.72			ns	8	3,5
T28	Data Strobe 'n' (DSTBP#) Output Valid Delay	1.25		3.55	ns	8	8
T29	First Data Strobe to Subsequent Strobe			2.5	ns	8	
T30	Data Input Setup Time to BCLK	.63			ns	9	7,9
T31	Data Input Setup Time to Strobe	0.34			ns	9	4
T32	Data Input Hold Time to Strobe	0.34			ns	9	4

Table 4-14. 533 MHz FSB Source Synchronous AC Specifications

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT	FIGURE	NOTES[1,2,3]
T17	Address Output Delay (first address only)	0.0		1.80	ns	6	3
T18	Address Output Valid Before Strobe	0.59			ns	6	3,5
T19	Address Output Valid After Strobe	0.59			ns	6	3,5
T20	Data Strobe 'N' (ASTBP#) Output Valid Delay	0.938		2.738	ns	6	8
T21	First Address Strobe to Subsequent Strobe			1.875	ns	6	
T22	Address Input Setup Time to BCLK	0.47			ns	7	7,9
T23	Address Input Setup Time to Strobe	0.22			ns	7	4
T24	Address Input Hold Time to Strobe	0.22			ns	7	4
T25	Data Output Delay (first data only)	0.0		1.80	ns	8	3
T26	Data Output Valid Before Strobe	0.59			ns	8	3,5
T27	Data Output Valid After Strobe	0.59			ns	8	3,5
T28	Data Strobe 'n' (DSTBP#) Output Valid Delay	0.938		2.738	ns	8	8
T29	First Data Strobe to Subsequent Strobe			1.875	ns	8	
T30	Data Input Setup Time to BCLK	0.47			ns	9	7,9
T31	Data Input Setup Time to Strobe	0.22			ns	9	4
T32	Data Input Hold Time to Strobe	0.22			ns	9	4

Table 4-15. 667 MHz FSB Source Synchronous AC Specifications

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT	FIGURE	NOTES[1,2,3]
T17	Address Output Delay (first address only)	0.0		1.25	ns	6	3
T18	Address Output Valid Before Strobe	0.55			ns	6	3,5
T19	Address Output Valid After Strobe	0.55			ns	6	3,5
T20	Data Strobe 'N' (ASTBP#) Output Valid Delay	0.75		2.00	ns	6	8
T21	First Address Strobe to Subsequent Strobe			1.5	ns	6	
T22	Address Input Setup Time to BCLK	0.38			ns	7	7,9
T23	Address Input Setup Time to Strobe	0.22			ns	7	4
T24	Address Input Hold Time to Strobe	0.22			ns	7	4
T25	Data Output Delay (first data only)	0.0		1.25	ns	8	3
T26	Data Output Valid Before Strobe	0.55			ns	8	3,5
T27	Data Output Valid After Strobe	0.55			ns	8	3,5
T28	Data Strobe 'n' (DSTBP#) Output Valid Delay	0.75		2.00	ns	8	8
T29	First Data Strobe to Subsequent Strobe			1.5	ns	8	
T30	Data Input Setup Time to BCLK	0.38			ns	9	7,9
T31	Data Input Setup Time to Strobe	0.22			ns	9	4
T32	Data Input Hold Time to Strobe	0.22			ns	9	4

Notes:

1. Guaranteed by design and not 100% tested.
2. All source synchronous AC timings are referenced to their associated strobe at 2/3 VCCP. Source synchronous data signals are referenced to the falling edge of their associated data strobe. Source synchronous address signals are referenced to the rising and falling edge of their associated address strobe. All source synchronous signal timings are referenced to 2/3 VCCP at the processor pad.
3. Valid delay timings for these signals are specified into the test circuit described in Figure 4-4 and at 2/3 VCCP.
4. Timing measured at 2/3 VCCP and assumes a slew rate between 1.0V/ns to 4.0V/ns.
5. The minimum time the data or address will be valid before its strobe.
6. The minimum time the data or address will be valid after its strobe.
7. N, which can be 0,1,2, or 3, refers to the strobe signals in each data group.
8. This specification applies only to DSTBP[3:0]# and is measured to the first falling edge of the strobe.
9. All source synchronous signals must meet the specified setup time to BCLK as well as the setup time to each respective strobe.
10.

Figure 4-9. Power Up Sequence

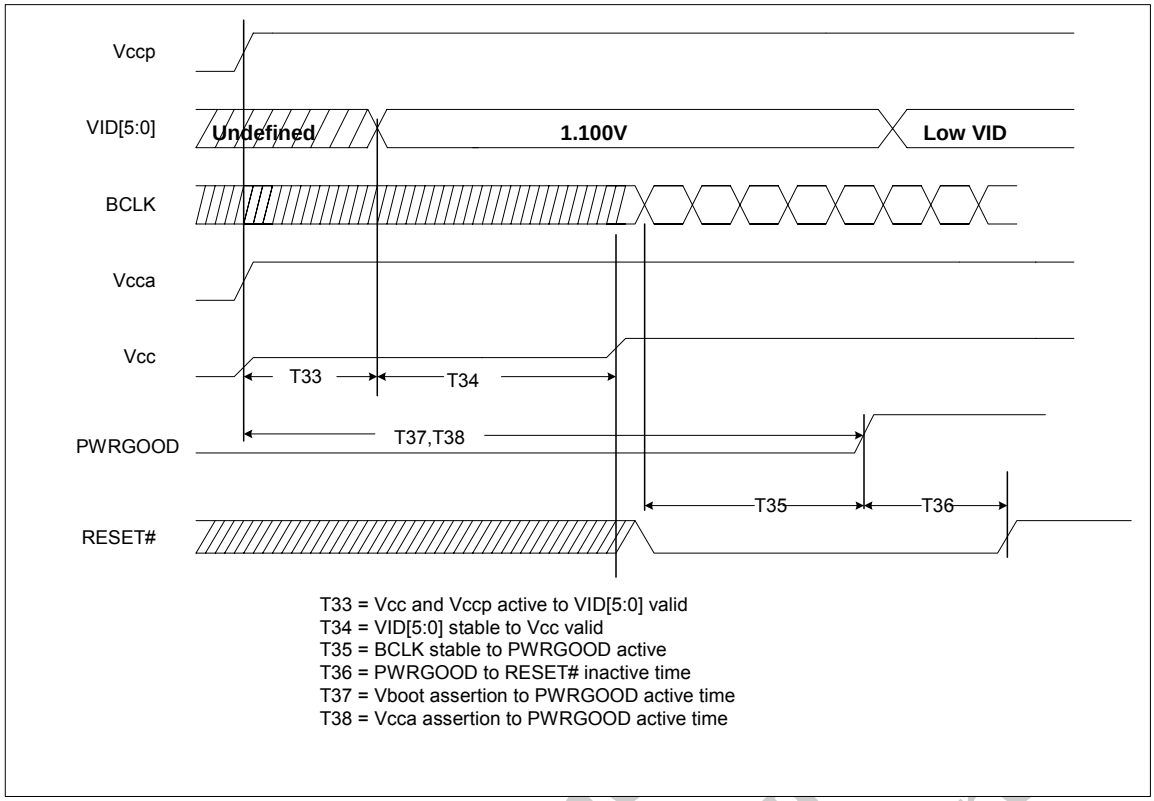


Figure 4-10. Power Down Sequence

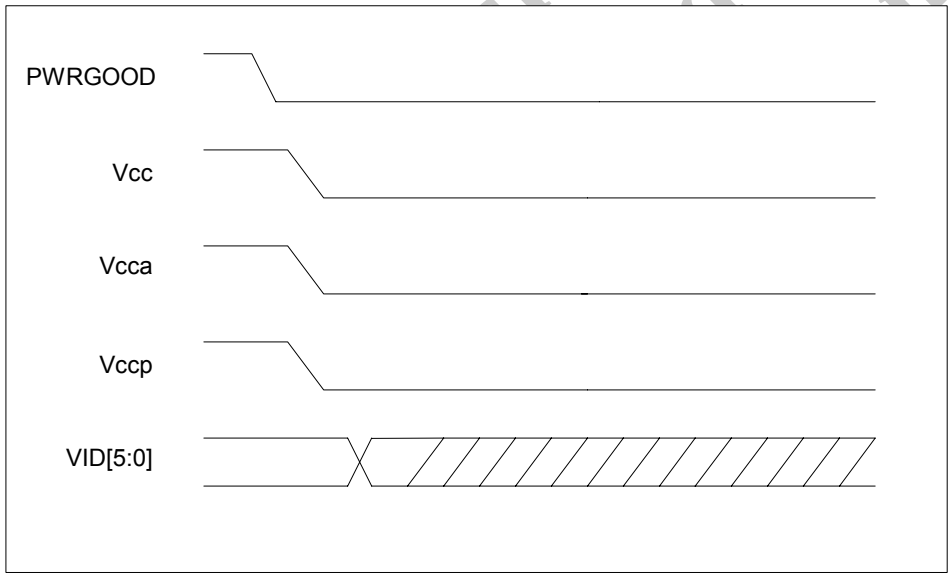


Figure 4-11. PROCHOT# Timings

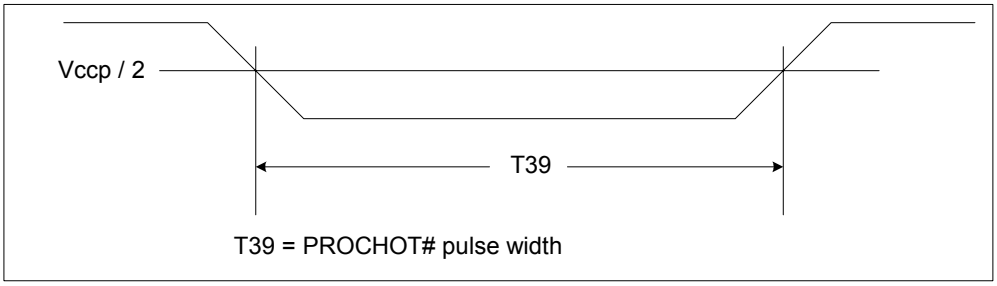


Figure 4-12. FERR# Break Event Timing

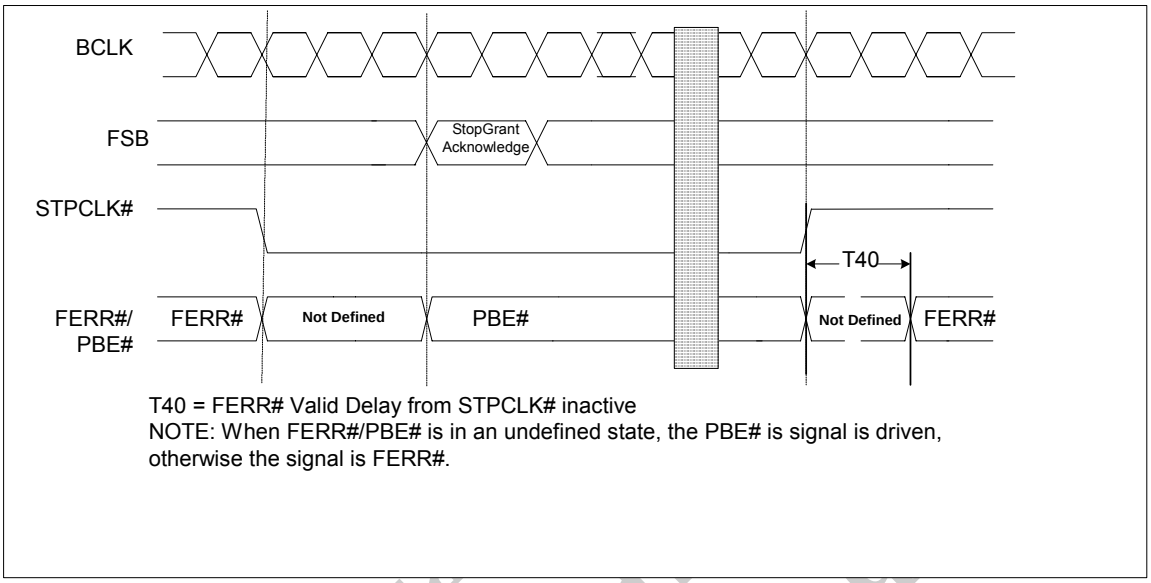


Figure 4-13. THERMTRIP# Assertion to Vcc Turn Off Timing

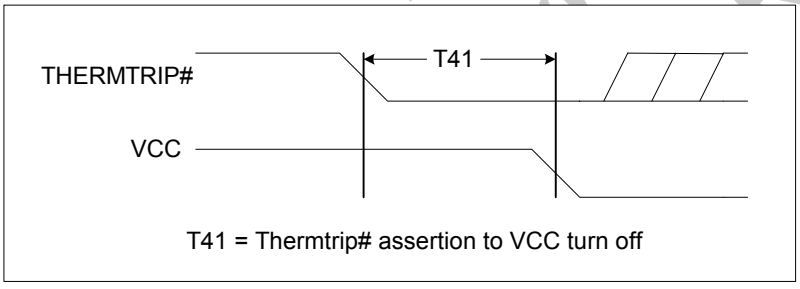


Table 4-16. CMOS Signal and Power Up AC Specifications

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES[1]
	CMOS Input Pulse Width, except PWRGOOD	3		BCLKs		
T33	V_{CC} & V_{CCP} assertion to VID valid		10	µs	9	5
T34	VID stable to V_{CC} valid		100	µs	9	
T35	BCLK stable to PWRGOOD assertion	10		BCLKs	9, 14	
T36	PWRGOOD to RESET# de-assertion time	2	10	ms	9, 14	
T36A	PWRGOOD rise time		50	ns	9, 14	4
T37	V_{BOOT} valid to PWRGOOD assertion	10		µs	9	
T38	V_{CCA} assertion to PWRGOOD assertion	2		µs	9	
T39	PROCHOT# pulse width	500		µs	11	3
T40	FERR# Valid Delay from STPCLK# de-assertion	0	5	BCLKs	12	
T41	THERMTRIP# assertion to Vcc turn off		500	ms	13	

Notes:

1. All CMOS signal timings are reference to VCCP/2.
2. CMOS signals are asynchronous in nature.
3. PROCHOT# assertion may not be exactly synchronized with thermal monitor enable.
4. Measured between 0.3*VCCP and 0.7*VCCP.
5. Defined as the time other system circuits can sample the VID signals.

Figure 4-14. FSB Reset and Configuration Timings

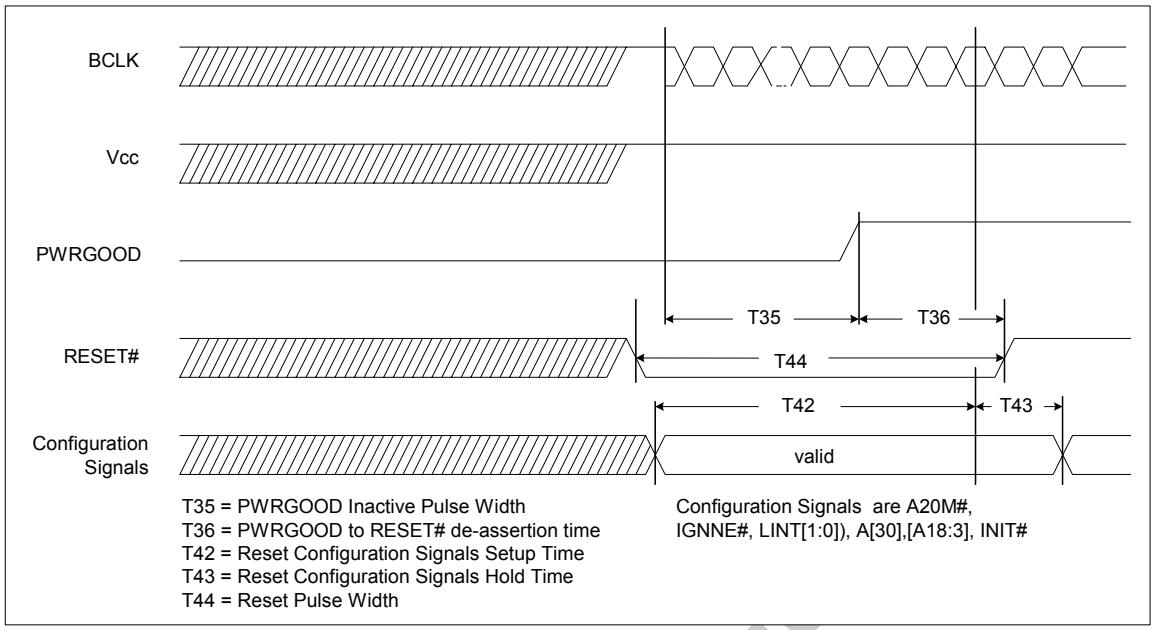


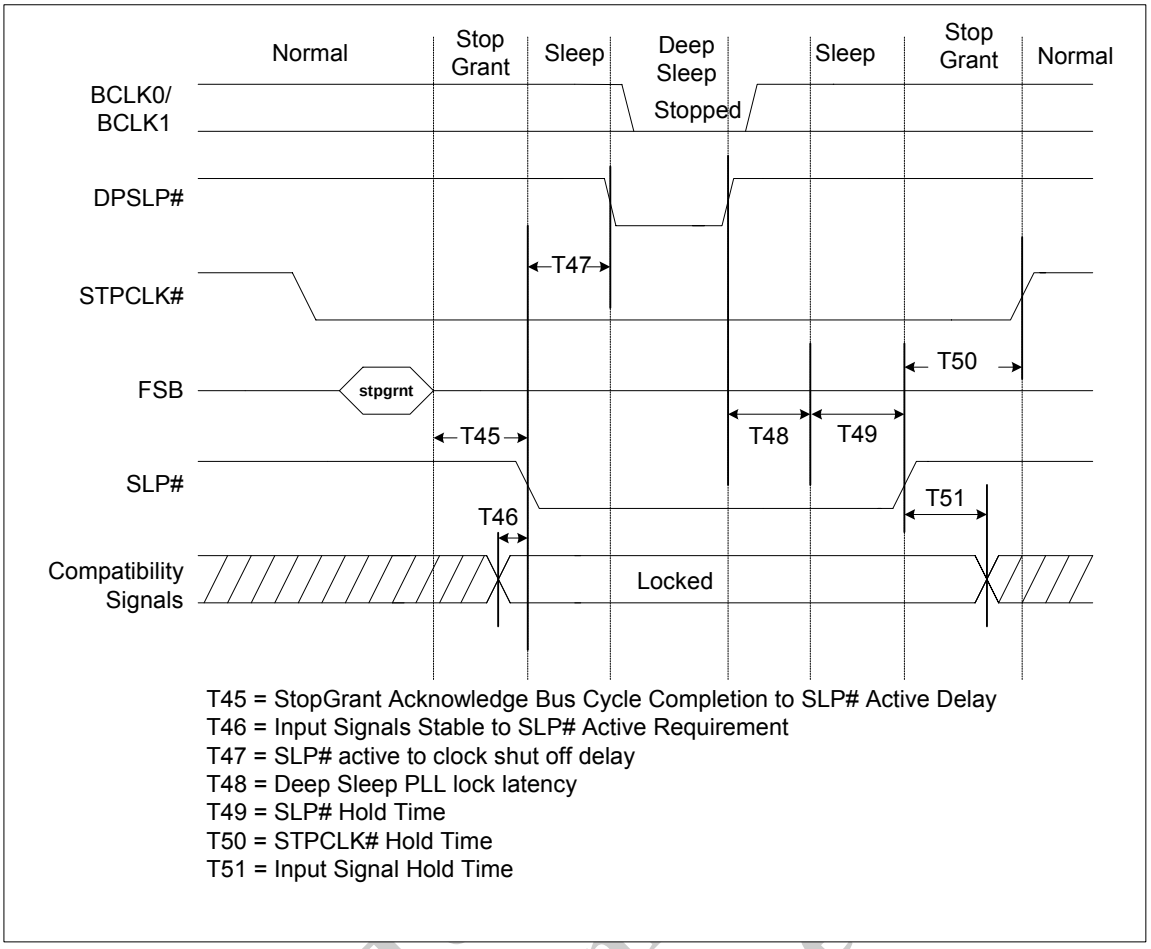
Table 4-17. FSB Reset Conditions

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
T42	Reset Configuration Signals Setup Time	1		µs	14	1
T43	Reset Configuration Signals Hold Time	2	20	BCLKs	14	2
T44	RESET# Pulse Width	0.015	100	ms	14	3,4,5

Notes:

1. Before the de-assertion of RESET#.
2. After clock that de-asserts RESET#.
3. RESET# can be asserted asynchronously, but must be deasserted synchronously.
4. This should be measured after VCCP and BCLK[1:0] become stable.
5. Maximum specification applies only while PWRGOOD is asserted.

Figure 4-15. Stop Grant/Sleep/Deep Sleep Timings



T45 = StopGrant Acknowledge Bus Cycle Completion to SLP# Active Delay
T46 = Input Signals Stable to SLP# Active Requirement
T47 = SLP# active to clock shut off delay
T48 = Deep Sleep PLL lock latency
T49 = SLP# Hold Time
T50 = STPCLK# Hold Time
T51 = Input Signal Hold Time

Table 4-18. Stop Grant/Sleep/Deep Sleep AC Specifications

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES[1]
T45	SLP# Signal Hold Time from Stop Grant Cycle Completion	10		BLCKs	15	
T46	Input Signals stable to SLP# assertion	2		BLCKs	15	
T47	SLP# assertion to DPSLP# assertion	2		BLCKs	15	
T48	Deep Sleep PLL Lock Latency		15	µs	15	
T49	SLP# Hold Time from PLL Lock	0		ns	15	
T50	STPCLK# Hold Time from SLP# de-assertion	2		BLCKs	15	
T51	Input Signal Hold Time from SLP# de-assertion	2		BLCKs	15	

Notes:

1. All input signals must maintain a constant state during sleep, except for RESET#.

Figure 4-16. JTAG Waveform

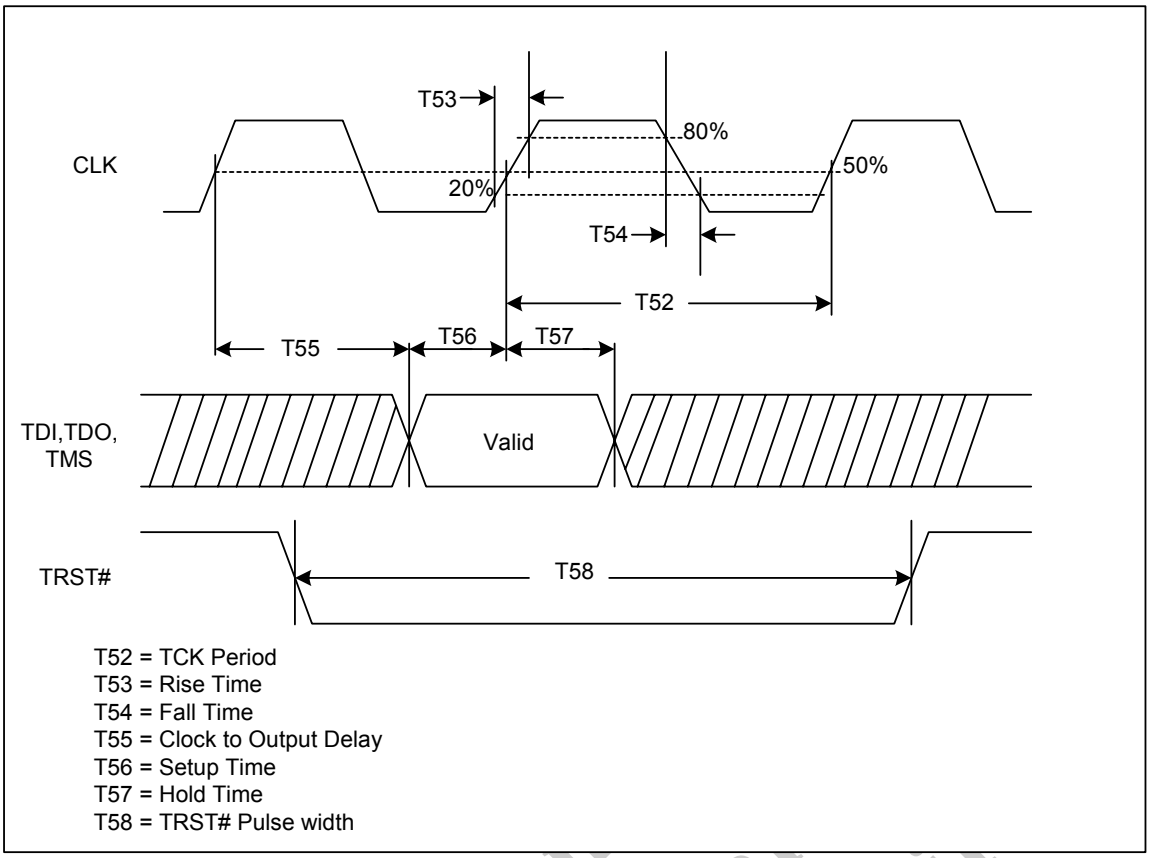


Table 4-19. JTAG AC Specifications

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT	FIGURE	NOTES[1]
T52	TCK Period	60			ns	16	
T52A	TCK Duty cycle	40		60	%		
T53	TCK Rise Time			10	ns	16	4
T54	TCK Fall Time			10	ns	16	4
T55	Clock to Output Delay			3.5	ns	16	6
T56	Setup Time	0			ns	16	5,7
T57	Hold Time	3			ns	16	5,7
T58	TRST# Assertion Time	2			TCK	16	8,9

Notes:

1. Guaranteed by design and not 100% tested.
2. AC timings for all JTAG signals are referenced to the TCK signal at 0.5 * Vccp at the processor pins.
3. Rise and fall times are measured from the 20% to 80% points of the signal swing.
4. Referenced to the rising edge of TCK.
5. Referenced to the falling edge of TCK.
6. Specifications for a minimum swing defined between Vccp V_{IL} and V_{IH}.
7. TRST# must be held active for 2 TCK periods to be guaranteed that it is recognized by the processor.
8. It is recommended that TMS be asserted while TRST# is being deactivated.

4.3 POWER DISSIPATION

Table 4-20 gives the core power consumption for the VIA C7 processor at the various operating frequencies and voltages. Note that this does not include the power consumed by the I/O pads.

Table 4-20. VIA C7 Thermal Design Power Information

	VIA C7 2.0 GHz				VIA C7 1.8 GHz			
Mode	**MHz**	**Voltage**	**Power (W)**	**Ratio & VID encoding (Hex)**	**MHz**	**Voltage**	**Power (W)**	**Ratio & VID encoding (Hex)**
Performance State P0	**2000**	**1.148**	**20**	141C	**1800**	**1.148**	**18**	121C
Performance State P1	800	0.956		0810	800	0.956		0810
HALT@50°C (C1)	2000 800	1.148 0.956	5.0 2.5		1800 800	1.148 0.956	5.0 2.5	
StopGrant@50°C (C2)	2000 800	1.148 0.956	5.0 2.5		1800 400	1.148 0.956	5.0 2.5	
Sleep@50°C	2000 800	1.148 0.956	4.5 2.0		1800 400	1.148 0.956	4.5 2.0	
DeepSleep@35°C (C3)	na	1.148 0.956	3.0 1.75		na	1.148 0.956	3.0 1.75	
DeeperSleep@35°C (C4)	na	0.748	0.5		na	0.748	0.5	

	VIA C7 1.6 GHz				VIA C7 1.5 GHz			
Mode	**MHz**	**Voltage**	**Power (W)**	**Ratio & VID encoding (Hex)**	**MHz**	**Voltage**	**Power (W)**	**Ratio & VID encoding (Hex)**
Performance State P0	**1600**	**1.084**	**15**	1018	**1500**	**1.004**	**12**	0F13
Performance State P1	800	0.956		0810	800	0.956		0810
HALT@50°C (C1)	1600 800	1.084 0.956	4.0 2.5		1500 800	1.004 0.956	3.5 2.5	
StopGrant@50°C (C2)	1600 800	1.084 0.956	4.0 2.5		1500 800	1.004 0.956	3.5 2.5	
Sleep@50°C	1600 800	1.084 0.956	3.5 2.0		1500 800	1.004 0.956	3.0 2.0	
DeepSleep@35°C (C3)	na	1.084 0.956	2.5 1.75		na	1.004 0.956	2.5 1.75	
DeeperSleep@35°C (C4)	na	0.748	0.5		na	0.748	0.5	

Table 4-21. VIA C7 Thermal Design Power Information

	VIA C7 1.0 GHz				VIA C7 1.3 GHz			
Mode	**MHz**	**Voltage**	**Power (W)**	**Ratio & VID encoding (Hex)**	**MHz**	**Voltage**	**Power (W)**	**Ratio & VID encoding (Hex)**
Performance State P0	**1000**	**1.004**	9	0A13	**1300**	**1.004**	12	0D13
Performance State P1	800	0.956		0810	800	0.956		0810
HALT@50°C (C1)	1000 800	1.004 0.956	3.5 2.5		1300 800	1.004 0.956	3.5 2.5	
StopGrant@50°C (C2)	1000 800	1.004 0.956	3.5 2.5		1300 800	1.004 0.956	3.5 2.5	
Sleep@50°C	1000 800	1.004 0.956	3.0 2.0		1300 800	1.004 0.956	3.0 2.0	
DeepSleep@35°C (C3)	na	1.004 0.956	2.5 1.75		Na	1.004 0.956	2.5 1.75	
DeeperSleep@35°C (C4)	na	0.748	0.5		Na	0.748	0.5	

	VIA C7 1.5 GHz			
Mode	**MHz**	**Voltage**	**Power (W)**	**Ratio & VID encoding (Hex)**
Performance State P0	**1500**	**1.084**	25	0F18
HALT@50°C (C1)	1500	1.084	7	
StopGrant@50°C (C2)	1500	1.084	7	
Sleep@50°C	1500	1.084	7	
DeepSleep@35°C (C3)	na	1.084	6	
DeeperSleep@35°C (C4)	na	0.748	2	

Notes:

1. Maximum power is generated from running publicly available application software that consumes the most power. Synthetic applications or "thermal virus" applications may consume more power.
2. The above power consumption is preliminary and based on 100°C junction temperature except as noted.
3. Conservative thermal solutions must be designed to account for worst-case core and I/O power consumption.

Table 4-22. V_{CCP} -I/O Power Consumption

PARAMETER	TYPICAL	MAX	UNITS	NOTES
PTT-I/O – I/O Operating Power Consumption	0.25	1.2	W	

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SECTION

5

MECHANICAL SPECIFICATIONS

5.1 NANOBGA2 PACKAGE

The VIA C7 processor is available in a very diminutive (21mm x 21mm) package, the nanoBGA2.

Figure 5-1. nanoBGA2 Ballout (Top View)

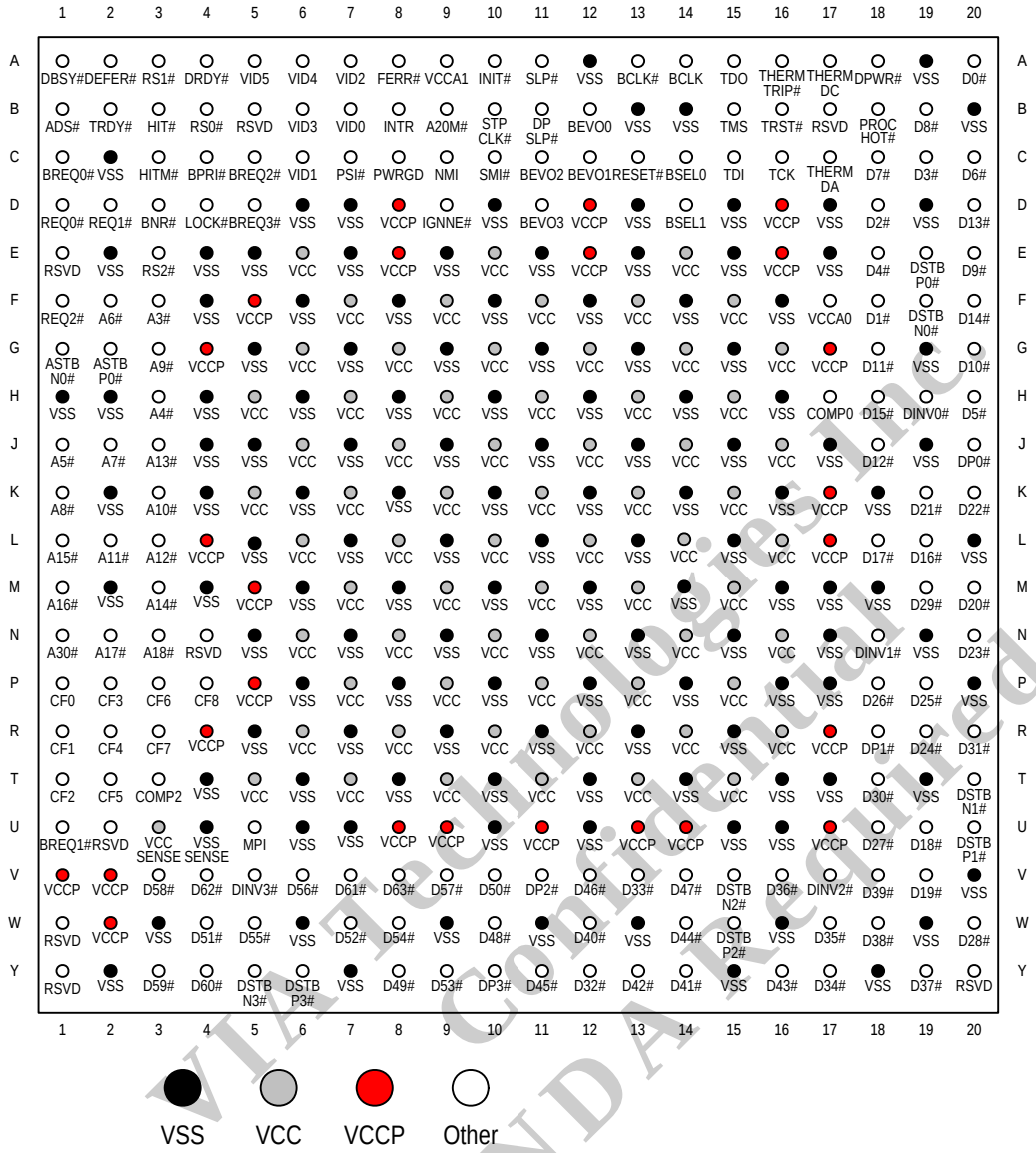

Table 5-1. Signal Listing in Order by Signal Name

Ball Name	Ball No	Type
A3#	F3	Source_Synch
A4#	H3	Source_Synch
A5#	J1	Source_Synch
A6#	F2	Source_Synch
A7#	J2	Source_Synch
A8#	K1	Source_Synch
A9#	G3	Source_Synch
A10#	K3	Source_Synch
A11#	L2	Source_Synch
A12#	L3	Source_Synch
A13#	J3	Source_Synch
A14#	M3	Source_Synch
A15#	L1	Source_Synch
A16#	M1	Source_Synch
A17#	N2	Source_Synch
A18#	N3	Source_Synch
A20M#	B9	CMOS
A30#	N1	Source_Synch
ADS#	B1	Common_Clock
ADSTBN0#	G1	Source_Synch
ADSTBP0#	G2	Source_Synch
BCLK	A14	Bus_Clock
BCLK#	A13	Bus_Clock
BEVO0	B12	CMOS
BEVO1	C12	CMOS
BEVO2	C11	CMOS
BEVO3	D11	CMOS
BNR#	D3	Common_Clock
BPRI#	C4	Common_Clock
BREQ0#	C1	Common_Clock
BREQ1#	U1	Common_Clock
BREQ2#	C5	Common_Clock
BREQ3#	D5	Common_Clock
BSEL0	C14	CMOS
BSEL1	D14	CMOS
CF0	P1	Power/Other
CF1	R1	Power/Other
CF2	T1	Power/Other
CF3	P2	Power/Other

Ball Name	Ball No	Type
CF4	R2	Power/Other
CF5	T2	Power/Other
CF6	P3	Power/Other
CF7	R3	Power/Other
CF8	P4	Power/Other
COMP0	H17	Power/Other
COMP2	T3	Power/Other
D0#	A20	Source_Synch
D1#	F18	Source_Synch
D2#	D18	Source_Synch
D3#	C19	Source_Synch
D4#	E18	Source_Synch
D5#	H20	Source_Synch
D6#	C20	Source_Synch
D7#	C18	Source_Synch
D8#	B19	Source_Synch
D9#	E20	Source_Synch
D10#	G20	Source_Synch
D11#	G18	Source_Synch
D12#	J18	Source_Synch
D13#	D20	Source_Synch
D14#	F20	Source_Synch
D15#	H18	Source_Synch
D16#	L19	Source_Synch
D17#	L18	Source_Synch
D18#	U19	Source_Synch
D19#	V19	Source_Synch
D20#	M20	Source_Synch
D21#	K19	Source_Synch
D22#	K20	Source_Synch
D23#	N20	Source_Synch
D24#	R19	Source_Synch
D25#	P19	Source_Synch
D26#	P18	Source_Synch
D27#	U18	Source_Synch
D28#	W20	Source_Synch
D29#	M19	Source_Synch
D30#	T18	Source_Synch
D31#	R20	Source_Synch

Table 5-1. Signal Listing in Order by Signal Name (Continued)

Ball Name	Ball No	Type
D32#	Y12	Source_Synch
D33#	V13	Source_Synch
D34#	Y17	Source_Synch
D35#	W17	Source_Synch
D36#	V16	Source_Synch
D37#	Y19	Source_Synch
D38#	W18	Source_Synch
D39#	V18	Source_Synch
D40#	W12	Source_Synch
D41#	Y14	Source_Synch
D42#	Y13	Source_Synch
D43#	Y16	Source_Synch
D44#	W14	Source_Synch
D45#	Y11	Source_Synch
D46#	V12	Source_Synch
D47#	V14	Source_Synch
D48#	W10	Source_Synch
D49#	Y8	Source_Synch
D50#	V10	Source_Synch
D51#	W4	Source_Synch
D52#	W7	Source_Synch
D53#	Y9	Source_Synch
D54#	W8	Source_Synch
D55#	W5	Source_Synch
D56#	V6	Source_Synch
D57#	V9	Source_Synch
D58#	V3	Source_Synch
D59#	Y3	Source_Synch
D60#	Y4	Source_Synch
D61#	V7	Source_Synch
D62#	V4	Source_Synch
D63#	V8	Source_Synch
DBSY#	A1	Common_Clock
DEFER#	A2	Common_Clock
DINV0#	H19	Source_Synch
DINV1#	N18	Source_Synch
DINV2#	V17	Source_Synch
DINV3#	V5	Source_Synch
DP0#	J20	Source_Synch

Ball Name	Ball No	Type
DP1#	R18	Source_Synch
DP2#	V11	Source_Synch
DP3#	Y10	Source_Synch
DPSLP#	B11	CMOS
DPWR#	A18	Common_Clock
DRDY#	A4	Common_Clock
DSTBN0#	F19	Source_Synch
DSTBN1#	T20	Source_Synch
DSTBN2#	V15	Source_Synch
DSTBN3#	Y5	Source_Synch
DSTBP0#	E19	Source_Synch
DSTBP1#	U20	Source_Synch
DSTBP2#	W15	Source_Synch
DSTBP3#	Y6	Source_Synch
FERR#	A8	Open_Drain
HIT#	B3	Common_Clock
HITM#	C3	Common_Clock
IGNNE#	D9	CMOS
INIT#	A10	CMOS
INTR	B8	CMOS
LOCK#	D4	Common_Clock
MPI	U5	Power/Other
NMI	C9	CMOS
PROCHOT#	B18	Open_Drain
PSI#	C7	CMOS
PWRGOOD	C8	CMOS
REQ0#	D1	Source_Synch
REQ1#	D2	Source_Synch
REQ2#	F1	Source_Synch
RESET#	C13	Common_Clock
RS0#	B4	Common_Clock
RS1#	A3	Common_Clock
RS2#	E3	Common_Clock
RSVD	B5	Reserved
RSVD	B17	Reserved
RSVD	E1	Reserved
RSVD	N4	Reserved
RSVD	U2	Reserved
RSVD	W1	Reserved

Table 5-1. Signal Listing in Order by Signal Name (Continued)

Ball Name	Ball No	Type
RSVD	Y1	Reserved
RSVD	Y20	Reserved
SLP#	A11	CMOS
SMI#	C10	CMOS
STPCLK#	B10	CMOS
TCK	C16	CMOS
TDI	C15	CMOS
TDO	A15	Open_Drain
THERMDA	C17	Power/Other
THERMDC	A17	Power/Other
THERMTRIP#	A16	Open_Drain
TMS	B15	CMOS
TRDY#	B2	Common_Clock
TRST#	B16	CMOS
VCC	E6	Power/Other
VCC	E10	Power/Other
VCC	E14	Power/Other
VCC	F7	Power/Other
VCC	F9	Power/Other
VCC	F11	Power/Other
VCC	F13	Power/Other
VCC	F15	Power/Other
VCC	G6	Power/Other
VCC	G8	Power/Other
VCC	G10	Power/Other
VCC	G12	Power/Other
VCC	G14	Power/Other
VCC	G16	Power/Other
VCC	H5	Power/Other
VCC	H7	Power/Other
VCC	H9	Power/Other
VCC	H11	Power/Other
VCC	H13	Power/Other
VCC	H15	Power/Other
VCC	J6	Power/Other
VCC	J8	Power/Other
VCC	J10	Power/Other
VCC	J12	Power/Other
VCC	J14	Power/Other

Ball Name	Ball No	Type
VCC	J16	Power/Other
VCC	K5	Power/Other
VCC	K7	Power/Other
VCC	K9	Power/Other
VCC	K11	Power/Other
VCC	K13	Power/Other
VCC	K15	Power/Other
VCC	L6	Power/Other
VCC	L8	Power/Other
VCC	L10	Power/Other
VCC	L12	Power/Other
VCC	L14	Power/Other
VCC	L16	Power/Other
VCC	M7	Power/Other
VCC	M9	Power/Other
VCC	M11	Power/Other
VCC	M13	Power/Other
VCC	M15	Power/Other
VCC	N6	Power/Other
VCC	N8	Power/Other
VCC	N10	Power/Other
VCC	N12	Power/Other
VCC	N14	Power/Other
VCC	N16	Power/Other
VCC	P7	Power/Other
VCC	P9	Power/Other
VCC	P11	Power/Other
VCC	P13	Power/Other
VCC	P15	Power/Other
VCC	R6	Power/Other
VCC	R8	Power/Other
VCC	R10	Power/Other
VCC	R12	Power/Other
VCC	R14	Power/Other
VCC	R16	Power/Other
VCC	T5	Power/Other
VCC	T7	Power/Other
VCC	T9	Power/Other
VCC	T11	Power/Other

Table 5-1. Signal Listing in Order by Signal Name (Continued)

Ball Name	Ball No	Type
VCC	T13	Power/Other
VCC	T15	Power/Other
VCCA0	F17	Power/Other
VCCA1	A9	Power/Other
VCCP	D8	Power/Other
VCCP	D12	Power/Other
VCCP	D16	Power/Other
VCCP	E8	Power/Other
VCCP	E12	Power/Other
VCCP	E16	Power/Other
VCCP	F5	Power/Other
VCCP	G4	Power/Other
VCCP	G17	Power/Other
VCCP	K17	Power/Other
VCCP	L4	Power/Other
VCCP	L17	Power/Other
VCCP	M5	Power/Other
VCCP	P5	Power/Other
VCCP	R4	Power/Other
VCCP	R17	Power/Other
VCCP	U8	Power/Other
VCCP	U9	Power/Other
VCCP	U11	Power/Other
VCCP	U13	Power/Other
VCCP	U14	Power/Other
VCCP	U17	Power/Other
VCCP	V1	Power/Other
VCCP	V2	Power/Other
VCCP	W2	Power/Other
VCC SENSE	U3	Power/Other
VID0	B7	Power/Other
VID1	C6	Power/Other
VID2	A7	Power/Other
VID3	B6	Power/Other
VID4	A6	Power/Other
VID5	A5	Power/Other
VSS	A12	Power/Other
VSS	A19	Power/Other
VSS	B13	Power/Other

Ball Name	Ball No	Type
VSS	B14	Power/Other
VSS	B20	Power/Other
VSS	C2	Power/Other
VSS	D6	Power/Other
VSS	D7	Power/Other
VSS	D10	Power/Other
VSS	D13	Power/Other
VSS	D15	Power/Other
VSS	D17	Power/Other
VSS	D19	Power/Other
VSS	E2	Power/Other
VSS	E4	Power/Other
VSS	E5	Power/Other
VSS	E7	Power/Other
VSS	E9	Power/Other
VSS	E11	Power/Other
VSS	E13	Power/Other
VSS	E15	Power/Other
VSS	E17	Power/Other
VSS	F4	Power/Other
VSS	F6	Power/Other
VSS	F8	Power/Other
VSS	F10	Power/Other
VSS	F12	Power/Other
VSS	F14	Power/Other
VSS	F16	Power/Other
VSS	G5	Power/Other
VSS	G7	Power/Other
VSS	G9	Power/Other
VSS	G11	Power/Other
VSS	G13	Power/Other
VSS	G15	Power/Other
VSS	G19	Power/Other
VSS	H1	Power/Other
VSS	H2	Power/Other
VSS	H4	Power/Other
VSS	H6	Power/Other
VSS	H8	Power/Other
VSS	H10	Power/Other

Table 5-1. Signal Listing in Order by Signal Name (Continued)

Ball Name	Ball No	Type
VSS	H12	Power/Other
VSS	H14	Power/Other
VSS	H16	Power/Other
VSS	J4	Power/Other
VSS	J5	Power/Other
VSS	J7	Power/Other
VSS	J9	Power/Other
VSS	J11	Power/Other
VSS	J13	Power/Other
VSS	J15	Power/Other
VSS	J17	Power/Other
VSS	J19	Power/Other
VSS	K2	Power/Other
VSS	K4	Power/Other
VSS	K6	Power/Other
VSS	K8	Power/Other
VSS	K10	Power/Other
VSS	K12	Power/Other
VSS	K14	Power/Other
VSS	K16	Power/Other
VSS	K18	Power/Other
VSS	L5	Power/Other
VSS	L7	Power/Other
VSS	L9	Power/Other
VSS	L11	Power/Other
VSS	L13	Power/Other
VSS	L15	Power/Other
VSS	L20	Power/Other
VSS	M2	Power/Other
VSS	M4	Power/Other
VSS	M6	Power/Other
VSS	M8	Power/Other
VSS	M10	Power/Other
VSS	M12	Power/Other
VSS	M14	Power/Other
VSS	M16	Power/Other
VSS	M17	Power/Other
VSS	M18	Power/Other
VSS	N5	Power/Other
VSS	N7	Power/Other
VSS	N9	Power/Other
VSS	N11	Power/Other
VSS	N13	Power/Other
VSS	N15	Power/Other
VSS	N17	Power/Other
VSS	N19	Power/Other
VSS	P6	Power/Other
VSS	P8	Power/Other
VSS	P10	Power/Other
VSS	P12	Power/Other
VSS	P14	Power/Other
VSS	P16	Power/Other
VSS	P17	Power/Other
VSS	P20	Power/Other
VSS	R5	Power/Other
VSS	R7	Power/Other
VSS	R9	Power/Other
VSS	R11	Power/Other
VSS	R13	Power/Other
VSS	R15	Power/Other
VSS	T4	Power/Other
VSS	T6	Power/Other
VSS	T8	Power/Other
VSS	T10	Power/Other
VSS	T12	Power/Other
VSS	T14	Power/Other
VSS	T16	Power/Other
VSS	T17	Power/Other
VSS	T19	Power/Other
VSS	U6	Power/Other
VSS	U7	Power/Other
VSS	U10	Power/Other
VSS	U12	Power/Other
VSS	U15	Power/Other
VSS	U16	Power/Other
VSS	V20	Power/Other
VSS	W3	Power/Other
VSS	W6	Power/Other

Table 5-1. Signal Listing in Order by Signal Name (Continued)

VSS	W9	Power/Other
VSS	W11	Power/Other
VSS	W13	Power/Other
VSS	W16	Power/Other
VSS	W19	Power/Other
VSS	Y2	Power/Other
VSS	Y7	Power/Other
VSS	Y15	Power/Other
VSS	Y18	Power/Other
VSS SENSE	U4	Power/Other

Table 5-2. Signal Listing in Order by Ball Number

Ball Name	Ball No	Type
DBSY#	A1	Common_Clock
DEFER#	A2	Common_Clock
RS1#	A3	Common_Clock
DRDY#	A4	Common_Clock
VID5	A5	Power/Other
VID4	A6	Power/Other
VID2	A7	Power/Other
FERR#	A8	Open_Drain
VCCA1	A9	Power/Other
INIT#	A10	CMOS
SLP#	A11	CMOS
VSS	A12	Power/Other
BCLK#	A13	Bus_Clock
BCLK	A14	Bus_Clock
TDO	A15	Open_Drain
THERMTRIP#	A16	Open_Drain
THERMDC	A17	Power/Other
DPWR#	A18	Common_Clock
VSS	A19	Power/Other
D0#	A20	Source_Synch
ADS#	B1	Common_Clock
TRDY#	B2	Common_Clock
HIT#	B3	Common_Clock
RS0#	B4	Common_Clock
RSVD	B5	Reserved
VID3	B6	Power/Other
VID0	B7	Power/Other
INTR	B8	CMOS
A20M#	B9	CMOS
STPCLK#	B10	CMOS
DPSLP#	B11	CMOS
BEVO0	B12	CMOS
VSS	B13	Power/Other
VSS	B14	Power/Other
TMS	B15	CMOS
TRST#	B16	CMOS
RSVD	B17	Reserved
PROCHOT#	B18	Open_Drain
D8#	B19	Source_Synch

Ball Name	Ball No	Type
VSS	B20	Power/Other
BREQ0#	C1	Common_Clock
VSS	C2	Power/Other
HITM#	C3	Common_Clock
BPRI#	C4	Common_Clock
BREQ2#	C5	Common_Clock
VID1	C6	Power/Other
PSI#	C7	CMOS
PWRGOOD	C8	CMOS
NMI	C9	CMOS
SMI#	C10	CMOS
BEVO2	C11	CMOS
BEVO1	C12	CMOS
RESET#	C13	Common_Clock
BSEL0	C14	CMOS
TDI	C15	CMOS
TCK	C16	CMOS
THERMDA	C17	Power/Other
D7#	C18	Source_Synch
D3#	C19	Source_Synch
D6#	C20	Source_Synch
REQ0#	D1	Source_Synch
REQ1#	D2	Source_Synch
BNR#	D3	Common_Clock
LOCK#	D4	Common_Clock
BREQ3#	D5	Common_Clock
VSS	D6	Power/Other
VSS	D7	Power/Other
VCCP	D8	Power/Other
IGNNE#	D9	CMOS
VSS	D10	Power/Other
BEVO3	D11	CMOS
VCCP	D12	Power/Other
VSS	D13	Power/Other
BSEL1	D14	CMOS
VSS	D15	Power/Other
VCCP	D16	Power/Other
VSS	D17	Power/Other
D2#	D18	Source_Synch

Table 5-2. Signal Listing in Order by Ball Number (Continued)

Ball Name	Ball No	Type
VSS	D19	Power/Other
D13#	D20	Source_Synch
RSVD	E1	Reserved
VSS	E2	Power/Other
RS2#	E3	Common_Clock
VSS	E4	Power/Other
VSS	E5	Power/Other
VCC	E6	Power/Other
VSS	E7	Power/Other
VCCP	E8	Power/Other
VSS	E9	Power/Other
VCC	E10	Power/Other
VSS	E11	Power/Other
VCCP	E12	Power/Other
VSS	E13	Power/Other
VCC	E14	Power/Other
VSS	E15	Power/Other
VCCP	E16	Power/Other
VSS	E17	Power/Other
D4#	E18	Source_Synch
DSTBP0#	E19	Source_Synch
D9#	E20	Source_Synch
REQ2#	F1	Source_Synch
A6#	F2	Source_Synch
A3#	F3	Source_Synch
VSS	F4	Power/Other
VCCP	F5	Power/Other
VSS	F6	Power/Other
VCC	F7	Power/Other
VSS	F8	Power/Other
VCC	F9	Power/Other
VSS	F10	Power/Other
VCC	F11	Power/Other
VSS	F12	Power/Other
VCC	F13	Power/Other
VSS	F14	Power/Other
VCC	F15	Power/Other
VSS	F16	Power/Other
VCCA0	F17	Power/Other

Ball Name	Ball No	Type
D1#	F18	Source_Synch
DSTBN0#	F19	Source_Synch
D14#	F20	Source_Synch
ADSTBN0#	G1	Source_Synch
ADSTBP0#	G2	Source_Synch
A9#	G3	Source_Synch
VCCP	G4	Power/Other
VSS	G5	Power/Other
VCC	G6	Power/Other
VSS	G7	Power/Other
VCC	G8	Power/Other
VSS	G9	Power/Other
VCC	G10	Power/Other
VSS	G11	Power/Other
VCC	G12	Power/Other
VSS	G13	Power/Other
VCC	G14	Power/Other
VSS	G15	Power/Other
VCC	G16	Power/Other
VCCP	G17	Power/Other
D11#	G18	Source_Synch
VSS	G19	Power/Other
D10#	G20	Source_Synch
VSS	H1	Power/Other
VSS	H2	Power/Other
A4#	H3	Source_Synch
VSS	H4	Power/Other
VCC	H5	Power/Other
VSS	H6	Power/Other
VCC	H7	Power/Other
VSS	H8	Power/Other
VCC	H9	Power/Other
VSS	H10	Power/Other
VCC	H11	Power/Other
VSS	H12	Power/Other
VCC	H13	Power/Other
VSS	H14	Power/Other
VCC	H15	Power/Other
VSS	H16	Power/Other

Table 5-2. Signal Listing in Order by Ball Number (Continued)

Ball Name	Ball No	Type
COMP0	H17	Power/Other
D15#	H18	Source_Synch
DINV0#	H19	Source_Synch
D5#	H20	Source_Synch
A5#	J1	Source_Synch
A7#	J2	Source_Synch
A13#	J3	Source_Synch
VSS	J4	Power/Other
VSS	J5	Power/Other
VCC	J6	Power/Other
VSS	J7	Power/Other
VCC	J8	Power/Other
VSS	J9	Power/Other
VCC	J10	Power/Other
VSS	J11	Power/Other
VCC	J12	Power/Other
VSS	J13	Power/Other
VCC	J14	Power/Other
VSS	J15	Power/Other
VCC	J16	Power/Other
VSS	J17	Power/Other
D12#	J18	Source_Synch
VSS	J19	Power/Other
DP0#	J20	Source_Synch
A8#	K1	Source_Synch
VSS	K2	Power/Other
A10#	K3	Source_Synch
VSS	K4	Power/Other
VCC	K5	Power/Other
VSS	K6	Power/Other
VCC	K7	Power/Other
VSS	K8	Power/Other
VCC	K9	Power/Other
VSS	K10	Power/Other
VCC	K11	Power/Other
VSS	K12	Power/Other
VCC	K13	Power/Other
VSS	K14	Power/Other
VCC	K15	Power/Other

Ball Name	Ball No	Type
VSS	K16	Power/Other
VCCP	K17	Power/Other
VSS	K18	Power/Other
D21#	K19	Source_Synch
D22#	K20	Source_Synch
A15#	L1	Source_Synch
A11#	L2	Source_Synch
A12#	L3	Source_Synch
VCCP	L4	Power/Other
VSS	L5	Power/Other
VCC	L6	Power/Other
VSS	L7	Power/Other
VCC	L8	Power/Other
VSS	L9	Power/Other
VCC	L10	Power/Other
VSS	L11	Power/Other
VCC	L12	Power/Other
VSS	L13	Power/Other
VCC	L14	Power/Other
VSS	L15	Power/Other
VCC	L16	Power/Other
VCCP	L17	Power/Other
D17#	L18	Source_Synch
D16#	L19	Source_Synch
VSS	L20	Power/Other
A16#	M1	Source_Synch
VSS	M2	Power/Other
A14#	M3	Source_Synch
VSS	M4	Power/Other
VCCP	M5	Power/Other
VSS	M6	Power/Other
VCC	M7	Power/Other
VSS	M8	Power/Other
VCC	M9	Power/Other
VSS	M10	Power/Other
VCC	M11	Power/Other
VSS	M12	Power/Other
VCC	M13	Power/Other
VSS	M14	Power/Other

Table 5-2. Signal Listing in Order by Ball Number (Continued)

Ball Name	Ball No	Type
VCC	M15	Power/Other
VSS	M16	Power/Other
VSS	M17	Power/Other
VSS	M18	Power/Other
D29#	M19	Source_Synch
D20#	M20	Source_Synch
A30#	N1	Source_Synch
A17#	N2	Source_Synch
A18#	N3	Source_Synch
RSVD	N4	Reserved
VSS	N5	Power/Other
VCC	N6	Power/Other
VSS	N7	Power/Other
VCC	N8	Power/Other
VSS	N9	Power/Other
VCC	N10	Power/Other
VSS	N11	Power/Other
VCC	N12	Power/Other
VSS	N13	Power/Other
VCC	N14	Power/Other
VSS	N15	Power/Other
VCC	N16	Power/Other
VSS	N17	Power/Other
DINV1#	N18	Source_Synch
VSS	N19	Power/Other
D23#	N20	Source_Synch
CF0	P1	Power/Other
CF3	P2	Power/Other
CF6	P3	Power/Other
CF8	P4	Power/Other
VCCP	P5	Power/Other
VSS	P6	Power/Other
VCC	P7	Power/Other
VSS	P8	Power/Other
VCC	P9	Power/Other
VSS	P10	Power/Other
VCC	P11	Power/Other
VSS	P12	Power/Other
VCC	P13	Power/Other

Ball Name	Ball No	Type
VSS	P14	Power/Other
VCC	P15	Power/Other
VSS	P16	Power/Other
VSS	P17	Power/Other
D26#	P18	Source_Synch
D25#	P19	Source_Synch
VSS	P20	Power/Other
CF1	R1	Power/Other
CF4	R2	Power/Other
CF7	R3	Power/Other
VCCP	R4	Power/Other
VSS	R5	Power/Other
VCC	R6	Power/Other
VSS	R7	Power/Other
VCC	R8	Power/Other
VSS	R9	Power/Other
VCC	R10	Power/Other
VSS	R11	Power/Other
VCC	R12	Power/Other
VSS	R13	Power/Other
VCC	R14	Power/Other
VSS	R15	Power/Other
VCC	R16	Power/Other
VCCP	R17	Power/Other
DP1#	R18	Source_Synch
D24#	R19	Source_Synch
D31#	R20	Source_Synch
CF2	T1	Power/Other
CF5	T2	Power/Other
COMP2	T3	Power/Other
VSS	T4	Power/Other
VCC	T5	Power/Other
VSS	T6	Power/Other
VCC	T7	Power/Other
VSS	T8	Power/Other
VCC	T9	Power/Other
VSS	T10	Power/Other
VCC	T11	Power/Other
VSS	T12	Power/Other

Table 5-2. Signal Listing in Order by Ball Number (Continued)

Ball Name	Ball No	Type
VCC	T13	Power/Other
VSS	T14	Power/Other
VCC	T15	Power/Other
VSS	T16	Power/Other
VSS	T17	Power/Other
D30#	T18	Source_Synch
VSS	T19	Power/Other
DSTBN1#	T20	Source_Synch
BREQ1#	U1	Common_Clock
RSVD	U2	Reserved
VCC SENSE	U3	Power/Other
VSS SENSE	U4	Power/Other
MPI	U5	CMOS
VSS	U6	Power/Other
VSS	U7	Power/Other
VCCP	U8	Power/Other
VCCP	U9	Power/Other
VSS	U10	Power/Other
VCCP	U11	Power/Other
VSS	U12	Power/Other
VCCP	U13	Power/Other
VCCP	U14	Power/Other
VSS	U15	Power/Other
VSS	U16	Power/Other
VCCP	U17	Power/Other
D27#	U18	Source_Synch
D18#	U19	Source_Synch
DSTBP1#	U20	Source_Synch
VCCP	V1	Power/Other
VCCP	V2	Power/Other
D58#	V3	Source_Synch
D62#	V4	Source_Synch
DINV3#	V5	Source_Synch
D56#	V6	Source_Synch
D61#	V7	Source_Synch
D63#	V8	Source_Synch
D57#	V9	Source_Synch
D50#	V10	Source_Synch
DP2#	V11	Source_Synch

Ball Name	Ball No	Type
D46#	V12	Source_Synch
D33#	V13	Source_Synch
D47#	V14	Source_Synch
DSTBN2#	V15	Source_Synch
D36#	V16	Source_Synch
DINV2#	V17	Source_Synch
D39#	V18	Source_Synch
D19#	V19	Source_Synch
VSS	V20	Power/Other
RSVD	W1	Reserved
VCCP	W2	Power/Other
VSS	W3	Power/Other
D51#	W4	Source_Synch
D55#	W5	Source_Synch
VSS	W6	Power/Other
D52#	W7	Source_Synch
D54#	W8	Source_Synch
VSS	W9	Power/Other
D48#	W10	Source_Synch
VSS	W11	Power/Other
D40#	W12	Source_Synch
VSS	W13	Power/Other
D44#	W14	Source_Synch
DSTBP2#	W15	Source_Synch
VSS	W16	Power/Other
D35#	W17	Source_Synch
D38#	W18	Source_Synch
VSS	W19	Power/Other
D28#	W20	Source_Synch
RSVD	Y1	Reserved
VSS	Y2	Power/Other
D59#	Y3	Source_Synch
D60#	Y4	Source_Synch
DSTBN3#	Y5	Source_Synch
DSTBP3#	Y6	Source_Synch
VSS	Y7	Power/Other
D4#	Y8	Source_Synch
D53#	Y9	Source_Synch
DP3#	Y10	Source_Synch

Table 5-2. Signal Listing in Order by Ball Number (Continued)

Ball Name	Ball No	Type
D45#	Y11	Source_Synch
D32#	Y12	Source_Synch
D42#	Y13	Source_Synch
D41#	Y14	Source_Synch
VSS	Y15	Power/Other
D43#	Y16	Source_Synch
D34#	Y17	Source_Synch
VSS	Y18	Power/Other
D37#	Y19	Source_Synch
RSVD	Y20	Reserved

Figure 5-2. nanoBGA2 Dimensions

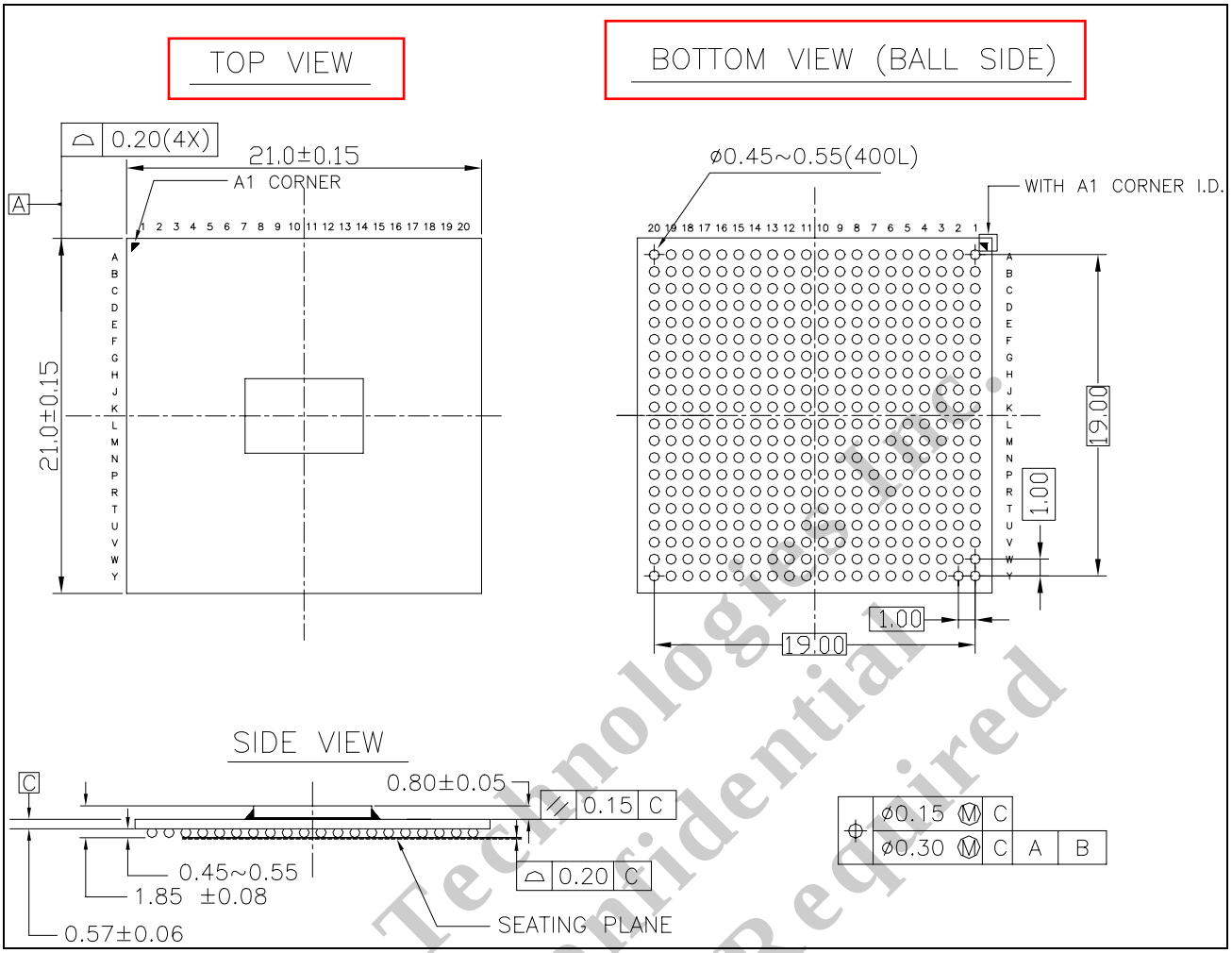

Table 5-3. Signal Listing in Order by Ball Number

Parameter	Measurement	Unit
Overall height, as delivered	1.85	mm
Die height	0.80	mm
Ball diameter	0.60	mm
Package substrate length	21.0±0.15	mm
Package substrate width	21.0±0.15	mm
Substrate thickness	0.57±0.06	mm
Ball pitch	1.00	mm
Ball count	400	--
Solder ball coplanarity	0.20	mm

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SECTION

6

THERMAL SPECIFICATIONS

6.1 INTRODUCTION

The VIA C7 is specified for operation with device case temperatures in the range of 0°C to 100°C. Operation outside of this range will result in functional failures and may potentially damage the device.

Care must be taken to ensure that the case temperature remains within the specified range at all times during operation. An effective heat sink with adequate airflow is therefore a requirement during operation.

6.2 TYPICAL ENVIRONMENTS

Typical thermal solutions involve three components: a heat sink, an interface material between the heat sink and the package, and a source of airflow. The best thermal solutions rely on the use of all three components. To the extent that any of these components are not used, the other components must be improved to compensate for such omission. In particular, the use of interface material such as thermal grease, silicone paste, or graphite paper can make a 40°C difference in the case temperature. Likewise, the imposition of airflow is realistically a requirement.

6.3 MEASURING T_C

The case temperature (T_C) should be measured by attaching a thermocouple to the center of the VIA C7 package. The heat produced by the processor is very localized so measuring the case temperature anywhere else will underestimate the case temperature.

The presence of a thermocouple is inherently invasive; effort must be taken to minimize the effect of the measurement. The thermocouple should be attached to the processor through a small hole drilled in the

heat sink. Thermal grease should be used to ensure that the thermocouple makes good contact with the package, but the thermocouple should not come in direct contact with the heat sink.

Physical Test Conditions

Case temperature measurements should be made in the worst case operating environments. Ideally, systems should be maximally configured, and tested at the worst-case ambient temperature.

Test Patterns

During normal operation the processor attempts to minimize power consumption. Consequently, normal power consumption is much lower than the maximum power consumption. Thermal testing should be done while running software which causes the processor to operate at its thermal limits.

6.4 MEASURING T_J

The junction temperature of the die can be measured by using the processor's on-chip diode.

6.5 ESTIMATING T_C

The VIA C7 processor's case temperature can be estimated based on the general characteristics of the thermal environment. This estimate is not intended as a replacement for actual measurement.

Case temperature can be estimated where,

$T_A \equiv$ Ambient Temperature

$T_C \equiv$ Case Temperature

$\theta_{CA} \equiv$ case-to-ambient thermal resistance

$\theta_{JA} \equiv$ junction-to-ambient thermal resistance

$\theta_{JC} \equiv$ junction-to-case thermal resistance ()

$P \equiv$ power consumption (Watts)

and,

The nanoBGA2 has θ_{JC} =0.2°C/W.

$T_J = T_C + (P * \theta_{JC})$

$T_A = T_J - (P * \theta_{JA})$

$T_A = T_C - (P * \theta_{CA})$

$\theta_{CA} = \theta_{JA} - \theta_{JC}$

6.6 THERMAL MONITOR

The VIA C7 processor provides an advanced mechanism for thermal management called the Thermal Monitor. In short, the processor has a second on-die thermal diode that is software accessible and allows a variety of actions based upon the current die temperature.

The processor will use a thermal feature when a pre-defined or user defined temperature threshold is met. The thermal feature will remain in use until the processor temperature is lowered as determined by the thermal monitor diode. Hysteresis is taken into account.

6.6.1 ON-DEMAND CLOCK MODULATION

On demand clock modulation allows the processor to assert an internal stop-clock duty cycle for thermal management. The throttling duty-cycle is user-defined.

See BIOS Writer's Guide for more details.

6.6.2 THERMAL MONITOR 1 AND THERMAL MONITOR 2

Thermal Monitor 1 or TM1 allows the processor to assert an internal power throttling state based upon pre-defined or user defined temperature thresholds. The throttling duty-cycle is pre-defined.

Thermal Monitor 2 or TM2 allows the processor to shift to a low-power performance state based upon pre-defined or user defined temperature thresholds. PowerSaver must be enabled for Thermal Monitor 2 to operate.

Thermal Monitor 1and Thermal Monitor 2 are mutually exclusive: system BIOS must choose which thermal protection mechanism to use. VIA strongly recommends the use of TM2 over TM1.

See BIOS Writer's Guide for more details.

6.6.3 APIC CONSIDERATIONS

The thermal monitor can generate an interrupt if the thermal monitor temperature threshold is tripped and the thermal entry is programmed into the processor's APIC LVT.

See BIOS Writer's Guide for more details.

6.6.4 USER DEFINED TEMPERATURE THRESHOLD

System designers may elect to use a specific trip point for thermal management.

Program the desired temperature in hexadecimal into MSR 0x1167.

SECTION

7

MACHINE SPECIFIC REGISTERS

7.1 GENERAL

Table 7-1 and Table 7-2 summarize the VIA C7 processor machine-specific registers (MSRs). Further description of each MSR follows the table. MSRs are read using the RDMSR instruction and written using the WRMSR instruction.

There are four basic groups of MSRs (not necessarily with contiguous addresses). Other than as defined below, a reference to an undefined MSR causes a General Protection exception.

1. Generally these registers can have some utility to low-level programs (like BIOS).

   Note that some of the MSRs (address 0 to 0x4FF) have no function in the VIA C7 processor. These MSRs do not cause a GP when used on the VIA C7 processor; instead, reads to these MSRs return zero, and writes are ignored. Some of these undocumented MSRs may have ill side effects when written to indiscriminately. Do not write to undocumented MSRs.

2. There are some undocumented internal-use MSRs used for low-level hardware testing purposes. Attempts to read or write these undocumented MSRs cause unpredictable and disastrous results; so don't use MSRs that are not documented in this datasheet.

3. MSRs used for cache and TLB testing. These use MSR addresses that are not used on compatible processor. These test functions are very low-level and complicated to use.

MSRs are not reinitialized by the bus INIT interrupt; the setting of MSRs is preserved across INIT.

Table 7-1. Category 1 MSRs

MSR	MSR NAME	ECX	EDX	EAX	TYPE	NOTES
TSC	Time Stamp Counter	10h	TSC[63:32]	TSC[31:0]	RW	
EBL_CR_POWERON	EBL_CR_POWERON	2Ah	n/a	Control bits	RW	
PERFCTR0	Performance counter 0	C1h	TSC[39:32]	TSC[31:0]	RW	1
PERFCTR1	Performance counter 1	C2h	0	Count[31:0]	RW	
BBL_CR_CTL3	L2 Hardware Disabled	11Eh	n/a	00800000h	RO	
EVNTSEL0	Event counter 0 select	186h	n/a	00470079h	RO	1
EVNTSEL1	Event counter 1 select	187h	n/a	Control bits	RW	
MTRR	MTRRphysBase0	200h	Control bits	Control bits	RW	
MTRR	MTRRphysMask0	201h	Control bits	Control bits	RW	
MTRR	MTRRphysBase1	202h	Control bits	Control bits	RW	
MTRR	MTRRphysMask1	203h	Control bits	Control bits	RW	
MTRR	MTRRphysBase2	204h	Control bits	Control bits	RW	
MTRR	MTRRphysMask2	205h	Control bits	Control bits	RW	
MTRR	MTRRphysBase3	206h	Control bits	Control bits	RW	
MTRR	MTRRphysMask3	207h	Control bits	Control bits	RW	
MTRR	MTRRphysBase4	208h	Control bits	Control bits	RW	
MTRR	MTRRphysMask4	209h	Control bits	Control bits	RW	
MTRR	MTRRphysBase5	20Ah	Control bits	Control bits	RW	
MTRR	MTRRphysMask5	20Bh	Control bits	Control bits	RW	
MTRR	MTRRphysBase6	20Ch	Control bits	Control bits	RW	
MTRR	MTRRphysMask6	20Dh	Control bits	Control bits	RW	
MTRR	MTRRphysBase7	20Eh	Control bits	Control bits	RW	
MTRR	MTRRphysMask7	20Fh	Control bits	Control bits	RW	
MTRR	MTRRfix64K_00000	250h	Control bits	Control bits	RW	
MTRR	MTRRfix16K_80000	258h	Control bits	Control bits	RW	
MTRR	MTRRfix16K_A0000	259h	Control bits	Control bits	RW	
MTRR	MTRRfix4K_C0000	268h	Control bits	Control bits	RW	
MTRR	MTRRfix4K_C8000	269h	Control bits	Control bits	RW	
MTRR	MTRRfix4K_D0000	26Ah	Control bits	Control bits	RW	
MTRR	MTRRfix4K_D8000	26Bh	Control bits	Control bits	RW	
MTRR	MTRRfix4K_E0000	26Ch	Control bits	Control bits	RW	
MTRR	MTRRfix4K_E8000	26Dh	Control bits	Control bits	RW	
MTRR	MTRRfix4K_F0000	26Eh	Control bits	Control bits	RW	
MTRR	MTRRfix4K_F8000	26Fh	Control bits	Control bits	RW	
MTRR	MTRRdefType	2FFh	Control bits	Control bits	RW	

Notes:

1. PERFCTR0 is an alias for the lower 40 bits of the Time Stamp Counter. EVNTSEL0 is a read only MSR that reflects this limitation.

Table 7-2. Category 2 MSRs

MSR	MSR NAME	ECX	EDX	EAX	TYPE	NOTES
FCR	Feature Control Reg	1107h	n/a	FCR value	RW	
FCR2	Feature Control Reg 2	1108h	FCR2_Hi	FCR2 value	RW	1
FCR3	Feature Control Reg 3	1109h	FCR3_Hi	FCR3 value	WO	1

Notes:

1. FCR2 and FCR3 provide system software with the ability to specify the Vendor ID string returned by the CPUID instruction.

7.2 CATEGORY 1 MSRS

10H: TSC (TIME STAMP COUNTER)

VIA C7 processor has a 64-bit MSR that materializes the Time Stamp Counter (TSC). System increments the TSC once per processor clock. The TSC is incremented even during AutoHalt or StopClock. A WRMSR to the TSC will clear the upper 32 bits of the TSC.

2AH: EBL_CR_POWERON

31:27	27	26	25:22	21:20	19:18	17:15	14	13	12:0
Res '11000'	BF4	Low-PowerEn '1'	BF[3:0]	*Res*	BSEL	*Res*	1MPOV	IOQDepth	*Reserved (Ignored on write; returns 0 on read)*
5	1	1	4	2	2	3	1	1	13

IOQDepth: 0 = In Order Queue Depth with up to 8 transactions
1 = 1 transaction

1MPOV: 0 = Power on Reset Vector at 0xFFFFFFF0 (4Gbytes)
1 = Power on Reset Vector at 0x000FFFF0 (1 Mbyte)

BSEL: 01 = 133 MHz Bus
10 = 100 MHz Bus

BF[4:0]: Core-to-Bus Frequency Ratio

Table 7-3. Core-to-Bus Frequency Ratio

Core Ratio	MSR 0x2A [27]	MSR 0x2A [25:22]
4	0	0100b
5	0	0101b
6	0	0110b
7	0	0111b
8	0	1000b
9	0	1001b
10	0	1010b
11	0	1011b
12	0	1100b
13	0	1101b
14	0	1110b
15	0	1111b
16	1	0000b
17	1	0001b
18	1	0010b
19	1	0011b
20	1	0100b
21	1	0101b
22	1	0110b
23	1	0111b
24	1	1000b
25	1	1001b

LowPowerEn: This bit always set to '1'

C1H-C2H: PERFCTR0 & PERFCTR1

These are events counters 0 and 1. VIA C7 processor's PERFCTR0 is an alias for the lower 40 bits of the TSC.

11EH: BBL_CR_CTL3

31:24	23	22:0
Reserved	L2_Hdw_Disable '1'	*Reserved* *(Ignored on write;* *returns 0 on read)*
8	1	23

The VIA C7 processor does contain an L2 cache. For compatibility, this read-only MSR indicates to the BIOS or system software that the L2 is disabled even if the L2 is enabled.

L2_Hdw_Disable: This bit always set to '1'

186H: EVNTSEL0 (EVENT COUNTER 0 SELECT)

31:24	23:16	15:9	8:0
Reserved	*Reserved*	*Reserved*	CTR0 Event Select = 79h
8	8	7	9

PERFCTR0 is an alias for the lower 40 bits of the Time Stamp Counter. EVNTSEL0 is a read only MSR which reflects this limitation. The CTR0_Event Select field always returns 0x0079, which corresponds to counting of processor clocks.

187H: EVNTSEL1 (EVENT COUNTER 1 SELECT)

31:24	23:16	15:9	8:0
Reserved	*Reserved*	*Reserved*	CTR1 Event Select
8	8	7	9

VIA C7 processor have two MSRs that contain bits defining the behavior of the two hardware event counters: PERFCTR0 and PERFCTR1.

The CTR1_Event_Select control field defines which of several possible events is counted. The possible Event Select values for PERFCTR1 are listed in the table below. Note that CTR1_Event_Select is a 9-bit field.

The EVNTSEL1 register should be written before PERFCTR1 is written to initialize the counter. The counts are not necessarily perfectly exact; the counters are intended for use over a large number of events and may differ by one or two counts from what might be expected.

Most counter events are internal implementation-dependent debug functions, having no meaning to software. The counters that can have end-user utility are:

EVENT	DESCRIPTION
C0h	Instructions executed
1C0h	Instructions executed and string iterations
79h	Internal clocks (default event for CTR0)

7.3 CATEGORY 2 MSRS

1107H: FCR (FEATURE CONTROL REGISTER)

The FCR controls the major optional feature capabilities of the VIA C7 processor. Table 7-4 contains the bit values for the FCR. The default settings shown for the FCR bits are not necessarily exact. The actual settings can be changed as part of the manufacturing process and thus a particular VIA C7 processor version can have slightly different default settings than shown here. All reserved bit values of the FCR must be preserved by using a read-modify-write sequence to update the FCR.

Table 7-4. FCR Bit Assignments

BIT	NAME	DESCRIPTION	DEFAULT
0	RSVD	*Reserved*	0
1	ECX8	Enables CPUID reporting CMPXCHG8B	1
7:2		*Reserved*	0
8	DL2	Disables L2 Cache	0
63:9		*Reserved*	0/1

ECX8: 0 = The CPUID instruction does not report the presence of the CMPXCHG8B instruction (CX8 = 0). The instruction actually exists and operates correctly, however.

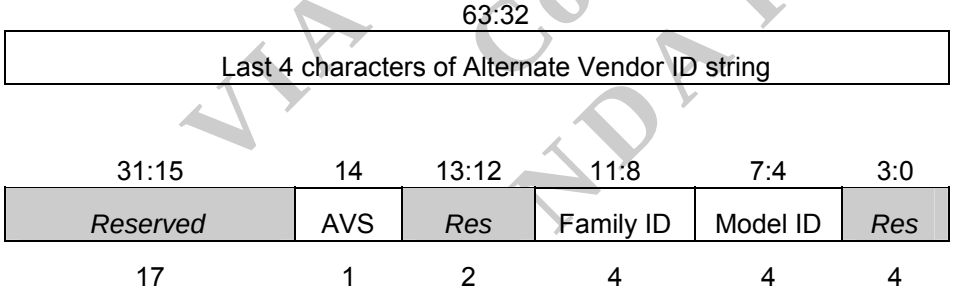
1 = The CPUID instruction reports that the CMPXCHG8B instruction is supported (CX8 = 1).

DL2: 0 = L2 Cache enabled.

1 = L2 Cache disabled.

1108H: FCR2 (FEATURE CONTROL REGISTER 2)

This MSR contains more feature control bits — many of which are undefined. It is important that all reserved bits are preserved by using a read-modify-write sequence to update the MSR.



AVS: 0 = The CPUID instruction vendor ID is "CentaurHauls"

1 = The CPUID instruction returns the alternate Vendor ID. The first 8 characters of the alternate Vendor ID are stored in FCR3 and the last 4 characters in FCR2[63:32]. These 12 characters are undefined after RESET and may be loaded by system software using WRMSR.

Family ID: This field will be returned as the family ID field by subsequent uses of the CPUID instruction

Model ID: This field will be returned as the model ID field by subsequent uses of the CPUID instruction

1109H: FCR3 (FEATURE CONTROL REGISTER 3)

This MSR contains the first 8 characters of the alternate Vendor ID. The alternate Vendor ID is returned by the CPUID instruction when FCR2[AVS] is set to '1'. FCR3 is a write-only MSR.

63:32
First 4 characters of Alternate Vendor ID string

31:0
Middle 4 characters of Alternate Vendor ID string